Emerging Interconnect Technologies

Prof. Krishna Saraswat

Department of Electrical Engineering
Stanford University, Stanford, CA, USA
Outline

• Scaling limits of interconnects
  ➢ Alternatives to Cu
• Performance simulations
  • Cu, CNT, optical interconnects
• Technology for novel optical interconnects
• 3-D integration
• Summary
Effect of Scaling on interconnect performance

Surface scattering

Barrier

Grain boundary scattering

Old

A

New (scaled)

$\text{Bit rate} \propto \frac{A}{l^2}$

$\text{Delay} \propto \frac{l^2}{A}$

$\text{Power dissipation} \sim CV^2f$
Graphene vs. TaN Barrier for Cu

Thinner barrier: 3.5 Å single layer graphene is better than 2 nm TaN

L. Li ... H.-S. P. Wong, Symp. VLSI Tech. 2015
L. Li ... H.-S. P. Wong, ACS Nano 2015
How can we improve interconnect performance?

- Carbon nanotubes/ Graphene
- Optical interconnects
- 3D
Optical & Electrical Wires: Schematic

On-chip Electrical Interconnect (Cu or CNT)

Driver → Repeater → Wire → Receiver

Off-chip Electrical Interconnect (Cu)

Driver → Wire → Receiver

Optical Interconnect

Transmitter System

laser source → Modulator → Optical signal → Waveguide

Input Electrical Signal → buffer chain (number of stage)

Laser/modulator converts electrical signal into optical signal

Receiver System

Waveguide → Photodetector

- Electrical

Rf (number of stage)

- Optical

TIR

Photodetector restores optical signal into electrical signal
Carbon Nanotubes

1-D conductors:

Quantum Wires:
- 1D system with limited density of states. Hence quantum effects play an important role in determining the values of R, L and C
- Mean free paths as large as 1.6µm.

3-D conductors:

Conventional wires:
- Backscattering through a series of small angle scatterings.
- Mean free paths ~ 30nm.

Potential Candidates for GSI Interconnects.
Formidable Task: Dense Bundles of SWNTs

Horizontal Growth for Interconnects
Y. Nishi and H.-S. Philip Wong (Stanford)

256-Element CNT Ring Oscillator
H.-S. Philip Wong (Stanford)

Vertical Growth
C.V. Thompson, MIT

Promising progress in creating aligned isolated SWNTs by transferring SWNTs grown on sapphire to other substrates
Potential reliability performance comparison

• Good thermal conductivity
  – Graphene: $4.84 \times 10^3 \sim 5.30 \times 10^3 W / mK$
  – CNT: $1.75 \times 10^3 \sim 5.80 \times 10^3 W / mK$
  – Copper: $385 W / mK$

• High breakdown current
  – Graphene: $\sim 10^8 A / cm^2$
  – CNT: $\sim 10^9 A / cm^2$
  – Copper (EM threshold): $\sim 10^7 A / cm^2$
Latency and Energy/bit vs. Wire Length

- Cu, CNT: small wire width → more repeaters, wire capacitance → latency ↑
- CNTs are favorable for shorter wires
- Optics favorable for longer wires

- Cu, CNT: small wire width → Energy per bit decreases as wire pitch is scaling (CV²)
- CNTs is favorable for shorter global wire
- Optics: transmitter receiver power ↓
- Optics favorable for longer wires

Comparison Study: Global Interconnect CNTs, Cu, Optics

- **BW density**
  
  Cu and CNTs: \( \frac{f_{\text{clk}}}{\text{pitch}_{\text{wire}}} \)
  
  Optics: no. of wavelength of WDM

- **Power density**
  
  Cu & CNTs (non-linear):
  
  Cap and wire pitch
  
  Optics (linear):
  
  no. of wavelength channel

- **Latency**
  
  Optics < CNTs < Cu

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Off-Chip Interconnect Performance: Electrical vs. Optical

- Beyond certain length optical I/O is more power efficient
- Critical length decreases at higher bit rate & lower detector capacitance
- Beyond 32nm Technology node critical length < 10cm
Why Really Photonics?

Source: Keren Bergman, Columbia University
Communication Dominates Power

On-Chip Power Breakdown
50nm node

- Signaling Interconnects (27%)
- Clock (28%)
- Memory (17%)
- Logic (27%)
- Latches
- Repeaters
- Distribution (Interconnects)

More than half the power can be attributed to interconnects

Chandra, Kapur and Saraswat, IEEE IITC, June 2002

70-80% of total logic power is for communication

- Need proper consideration of wires!!

Why Off-chip Photonic Interconnects

- Copper wires are reaching physical limits
- Photonic interconnects offer the solution for the future
The Interconnect Problem

“For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration … will deliver the solution” (ITRS)

Source: Intel
Material Options for Optical Interconnects

• What are the right optical devices to use?
  – Need to be cheap, available in large numbers
  – Compatible with CMOS

• Silicon devices are a long shot
  – Need 3D heterogeneous integration

• Flip bond III-V to Si CMOS
  – Current process
  – Cost, resources, yield?

• How about germanium?
  – Bandgap ideal for $\lambda = 1.5 \, \mu m$
  – Can be monolithically integrated on Si
  – Becomes direct bandgap material by straining or adding tin
Selective and Lateral Overgrowth of Ge on SiO₂

- Lateral Ge growth on SiO₂ window achieved
- Dislocation density of Ge on SiO₂ < 10⁶ cm⁻² (same thickness Ge on Si: 1×10⁸ /cm²)
- Surface RMS roughness ~0.4 nm after CMP
- Ge is ~0.2% tensile strained due to thermal mismatch with Si

Ju Hyung Nam...........K. Saraswat, J. Crystal Growth, April 2015
Si Compatible Photonic Interconnect

- Germanium devices can be monolithically integrated on silicon
- Laser is the only missing component

Laser/modulator converts electrical signal into optical signal

Photodetector restores optical signal into electrical signal

Laser Source -> Modulator -> Waveguide

Modulator

Photodetector

Receiver

Laser

Modulator

Waveguide

Detector

Germanium (Ge) devices can be monolithically integrated on silicon.

Laser is the only missing component.


Gupta......... Saraswat, OFC, March 2015

Okyay.......... Saraswat, Optics Lett. 2006
Technology for Optical Interconnects on Silicon: Optical Transmission Media

Waveguides

Bending Waveguides

Waveguide Crossings

Couplers

Splitter

[K. Xia et al., Nature Photonics, 2006]

[K. Bogaerts et al., Optics Letters, 2007]

(Kramerlingr, MIT)
High Efficiency Ge p-i-n Photodetectors on Si

- Ge grown on Si by **Multiple Hydrogen Anneal and Heteroepitaxy (MHAH) Technique**
- Ge film complies with Si substrate on cooling down resulting in tensile strain => bandgap reduces
- Detector efficiency improves at 1550nm due to tensile stress
- Dark Current high

Optical Modulator

**Electro-optic Modulators**
- Index change
- Weak mechanism
- High Q
- Temperature tuning

Lipson (Cornell)

**Mach-Zehnder Modulators**
- Phase shift effect in waveguides
- Large size and power consumption

**Electro-absorption Modulators**
- Saraswat (Stanford)
- Franz-Keldysh effect in bulk material

**QCSE Ge/SiGe Modulator**
- Harris and Miller (Stanford)
CHAPTER 1. INTRODUCTION

In the presence of an electric field, the conduction and valence bands of a semiconductor tilt. Application of an electric field leads to overlap in valence and conduction band wave functions, and hence optical absorption, at energies below the semiconductor bandgap.
Structure Needs for Efficient Lasing

For efficient laser

- Direct bandgap cavity
- Heterojunction quantum well for carrier confinement

E. F. Schubert, Light Emitting Diodes (Cambridge Univ. Press)
Engineering Ge for light emission - Doping

• N-type doping can be used to fill electrons into the L valley up to the level of Γ valley
• But it is difficult to heavily dope Ge n-type
• Increases free carrier absorption and auger recombination
• Inefficient light emission
Engineering the Ge band structure for light emission: Strain

>1.7% biaxial tensile strain or > 5% uniaxial tensile strain turns Ge into a direct bandgap material, making light emission possible

*Sukhdeo, ..... Saraswat, Photonics Research, 2014*
Heterostructure in a Single Material: Strained Ge

- Strain can be tunable with geometry
- Heterostructure created due to reduction in bandgap of strained Ge
- Direct bandgap cavity and hetrojunction quantum well in single material

Engineering the Ge band structure by alloying with tin for GeSn CMOS and photonics

$\text{Ge}_{1-x}\text{Sn}_x$ becomes direct band gap!

At ~ 7 Sn% $\text{Ge}_{1-x}\text{Sn}_x$ becomes direct band gap!

Gupta, Yeo, Takagi, Saraswat, et al., MRS Bulletin, Aug 2014

3-D IC: CMOS, Photonics co-integration
Demonstration of Optically Pumped GeSn Laser

- Lasing emission spectra measured from the facet of a 5 μm x1 mm long Fabry-Perot waveguide Ge$_{0.87}$Sn$_{0.13}$ cavity under optical pumping at 20 K.
- More work needed for room temperature laser
Direct Bandgap GeSn Microdisk Laser on a Si-Platform

- Power-dependent PL spectra of an 8 μm diameter Ge$_{0.875}$ Sn$_{0.125}$ microdisk at 50 K.
- More work needed for room temperature laser

S. Wirth, et al., IEEE IEDM, Dec. 2015
A combination of alloying Ge with Sn and strain can also give us a direct bandgap material

- Efficiency would be comparable to present III-V lasers

3-D Integration: Motivation

- Reduce Chip footprint
  - Improved form factor
  - Interconnect length ↓ and therefore R, L, C ↓
    - Delay reduction
    - Power reduction
    - Higher bandwidth

- Integration of heterogeneous technologies possible, e.g., memory & logic, sensors, optical I/O
Technology to Fabricate 2.5D/3D ICs

- **2.5D packaging** (mature technology)
  - Wire bonded
  - Bump
  - vertical interconnect density < 20/mm or 400/mm²

- **3D bonding/TSV** (emerging technology)
  - Die stacking
  - wafer stacking
  - vertical interconnect density < 40,000/mm²

- **3D crystallization** (near future technology)
  - Epitaxial growth
  - Laser melting and crystallization
  - Seeded crystallization
  - Liquid phase crystallization
  - vertical interconnect density < 25M/mm²

- **3D self assembled devices** (future technology)
  - Si and Ge nanowires
  - Carbon nanotubes
  - Organic semiconductors
Monolithic 3D Integration of Si MOSFETs with RRAMs and CNTFETs

Heterogeneous 3D Integration Faster than Moore

# of transistors/chip
(performance/functionality)

2008 2010 2012 2014

2-D Batch
Moore

45nm 32nm 22nm 15nm 11nm

Production year

3D Monolithic
3D Bonding
2.5D Packaging

Faster than Moore
Slower than Moore
Future Systems will Require Heterogeneous 3D Integration on a Si Platform

Metal interconnect

Conventional transistors

3D System

Novel transistors

Photonics

MEMS/Sensors

Bio devices

Heat Transfer

Memory
Conclusion

😊 Cu resistivity increases as technology scales down. This will be a bottleneck of future high-performance chip.

😊 CNTs have a significant advantage over Cu wires especially for local interconnects.

😊 Optical links have smallest latency and energy per bit for longer global interconnects requiring higher band width.

😊 3D heterogeneous integration will keep the Moore’s law going for awhile.
Contributors / Collaborators:

Hoyeol Cho, Raj Dutt, Shashank Gupta, Suyog Gupta, Jim Harris, Pawan Kapur, Kyung-Ho Koo, Donguk Nam, Ju Hyung Nam, Ammar Nayfeh, Ali Okyay, Jan Petykiewicz, Dave Sukhdeo, Jelena Vuckovic and Hyun-Yong Yu.