



# Pre SiGe Wet Cleans Development for sub 1x nm Technology Node

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## Background

- ❑ Due to higher aspect ratio features observed in advanced technology nodes (1x nm and smaller), the epi growth uniformity suffers across wafer
- ❑ Carbon, fluorine and oxygen residues incoming from post etch and ashing steps degrade the surface cleanliness and inhibit the epitaxial growth = missing epi defects
- ❑ Need C, O and F at low levels simultaneously going into epi deposition

## Objective

- ❑ Improve pre-Epi wet cleans to ensure a pristine surface suitable for uniform epitaxial growth
- ❑ Ensure wet cleans equipment is not contributing to WiW non-uniformity

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Achieving Pristine Wafer  
Surface with Pre-Epi  
Wet Clean

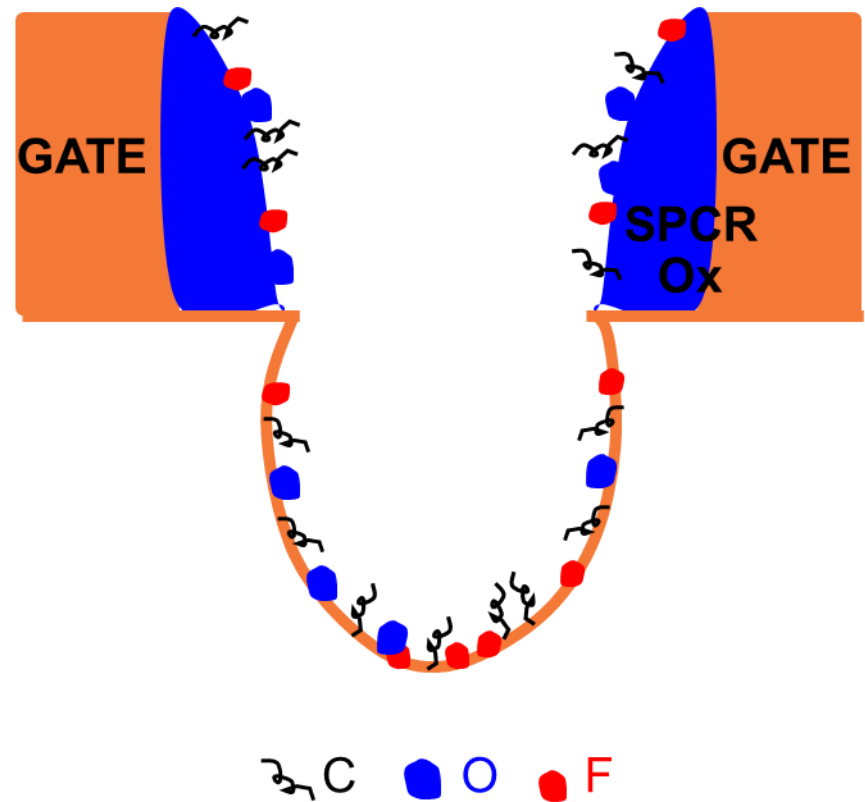
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Improving Cavity Size  
WiW Uniformity

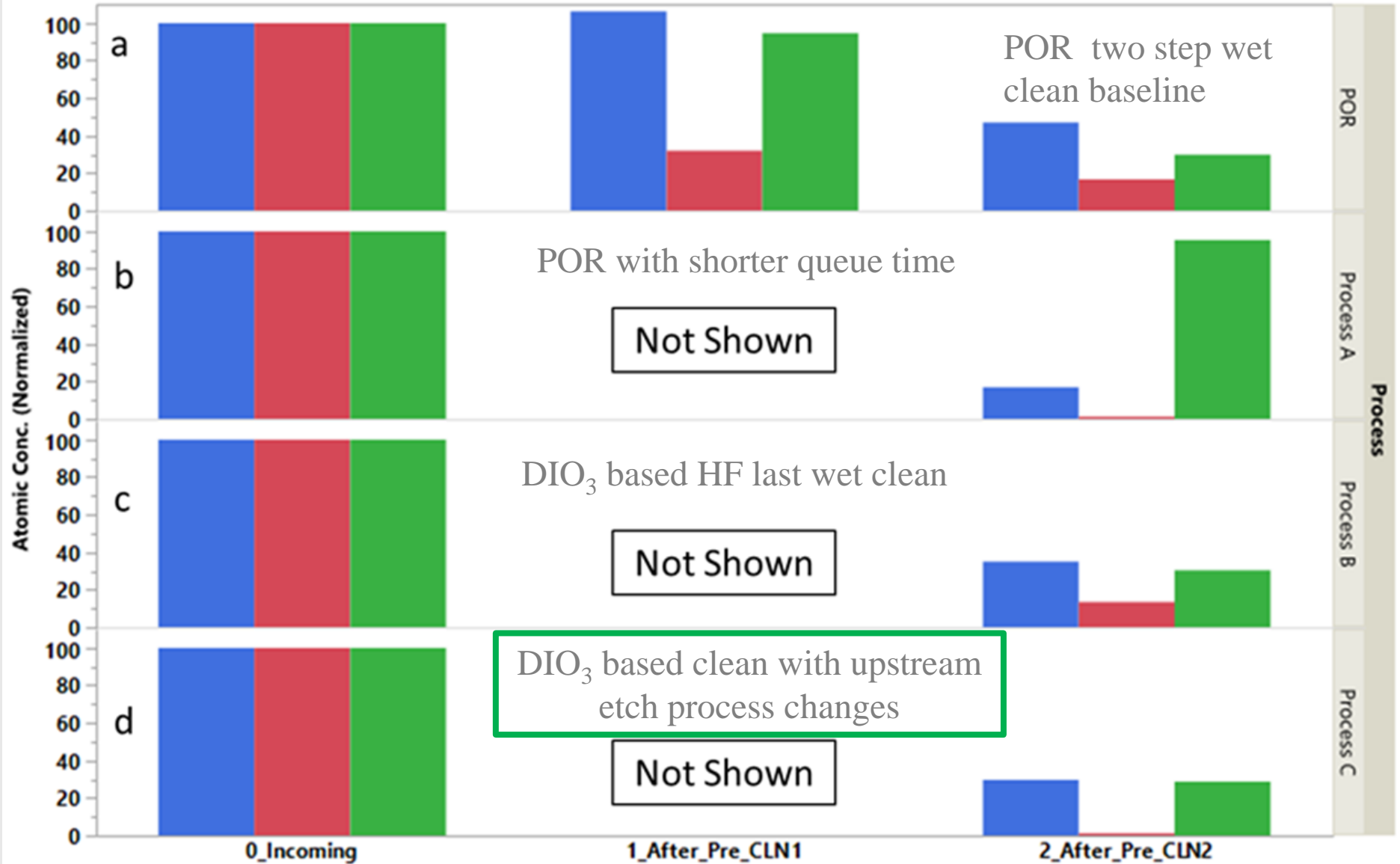


# Sub 1x nm HVM Requirements for Pre-EPI Wet Cleans

- ❑ POR wet cleans are two-step cleans (back to back)
- ❑ HVM Requirements:
  - ❑ Eliminate carbon, fluorine and oxygen residues from cavity and SPCR Ox
  - ❑ SPCR Ox loss is minimal (= limited dHF usage in wet clean steps)
  - ❑ Retain cavity shape and size
  - ❑ Zero WiW non-uniformity

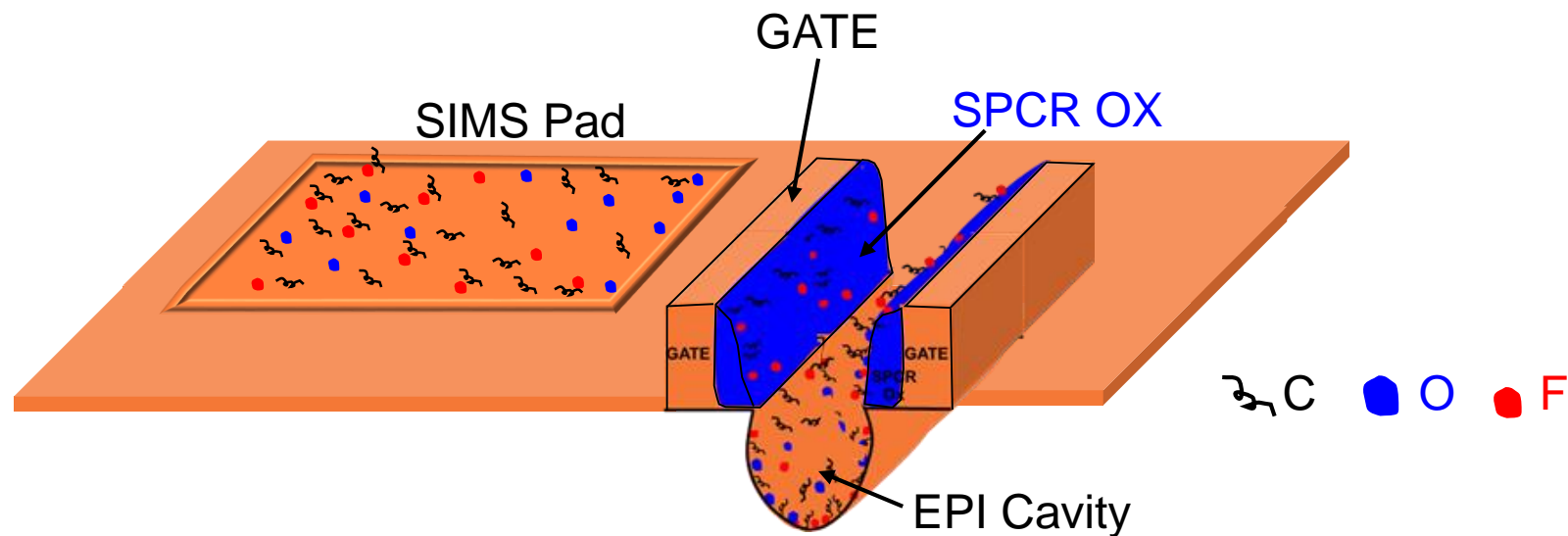


# Pre-EPI Wet Clean Splits and XPS Results



# Sub 1x nm HVM Requirements for Pre-EPI Wet Cleans

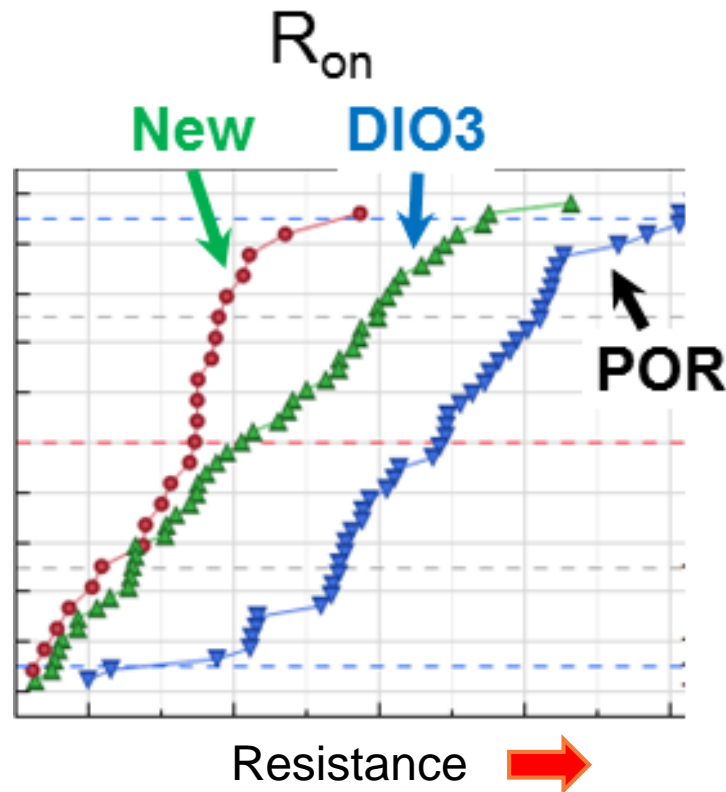
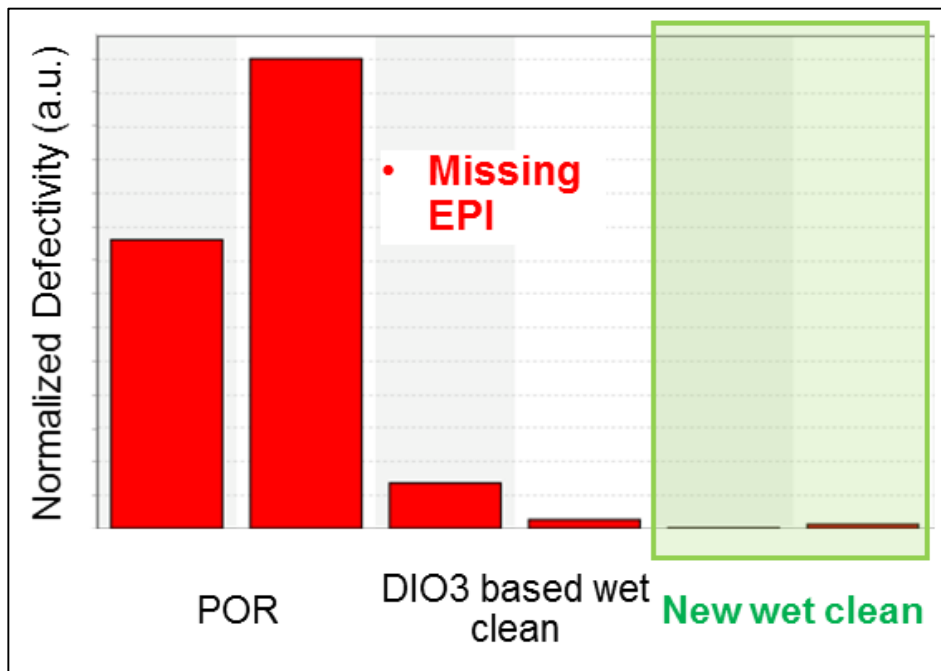
- ❑  $\text{DIO}_3$  based wet clean did not lower missing epi defectivity to required levels



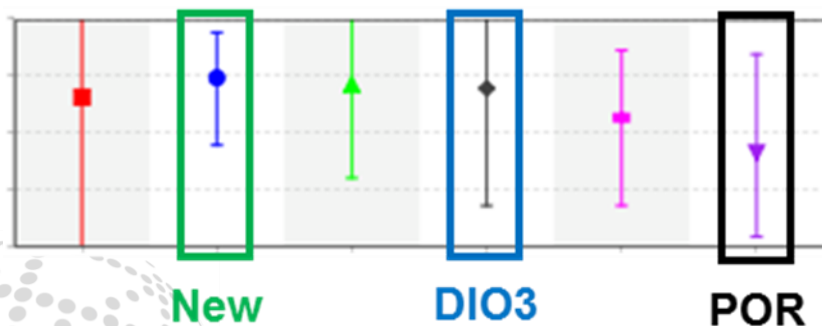
- ❑ SIMS pad measurements not reflective of C, O and F removal from SPCR Ox and epi cavity

➔ Therefore, we had to develop a new pre-epi wet clean

# Results from 1<sup>st</sup> Split Lot



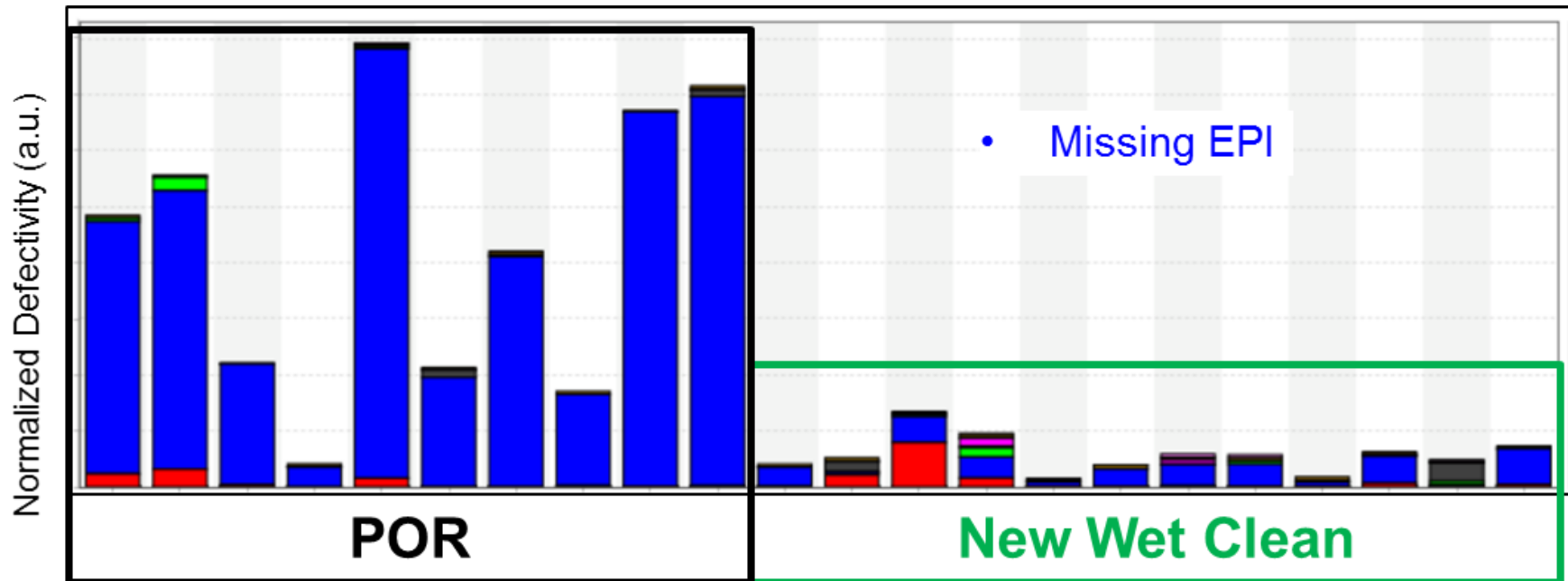
Cavity Size



- New pre-epi wet clean
- $R_{on} \downarrow$  to largest extent with New wet clean
- Cavity size is unchanged
- $\sim 50x \downarrow$  in missing epi defects

# Post Implementation Results

SPC chart for Missing Epi after implementation as POR



## □ New Pre-Epi Wet Clean

- Accomplished with no change in SPCR dimension from old POR
- Pristine wafer surface required additional changes in upstream processes
- Further optimization in progress



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Achieving Pristine Wafer  
Surface with Pre-Epi Wet Clean

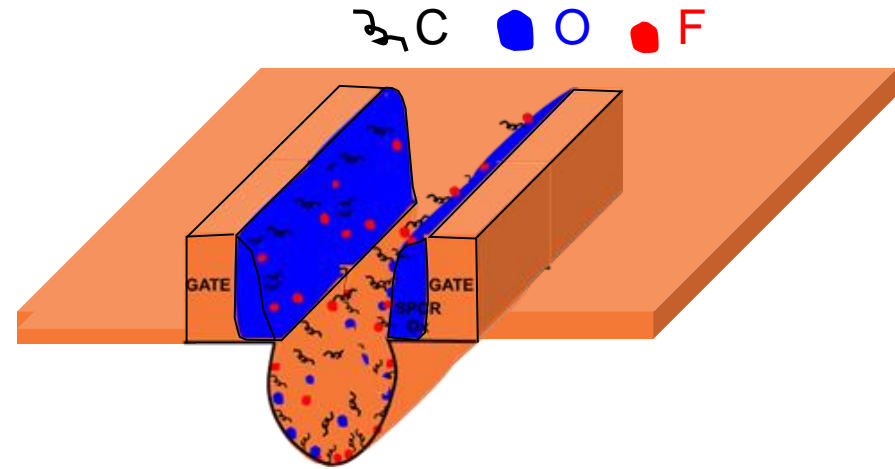
2

Improving Cavity Size  
WiW Uniformity



# Need for WiW Uniformity Improvement

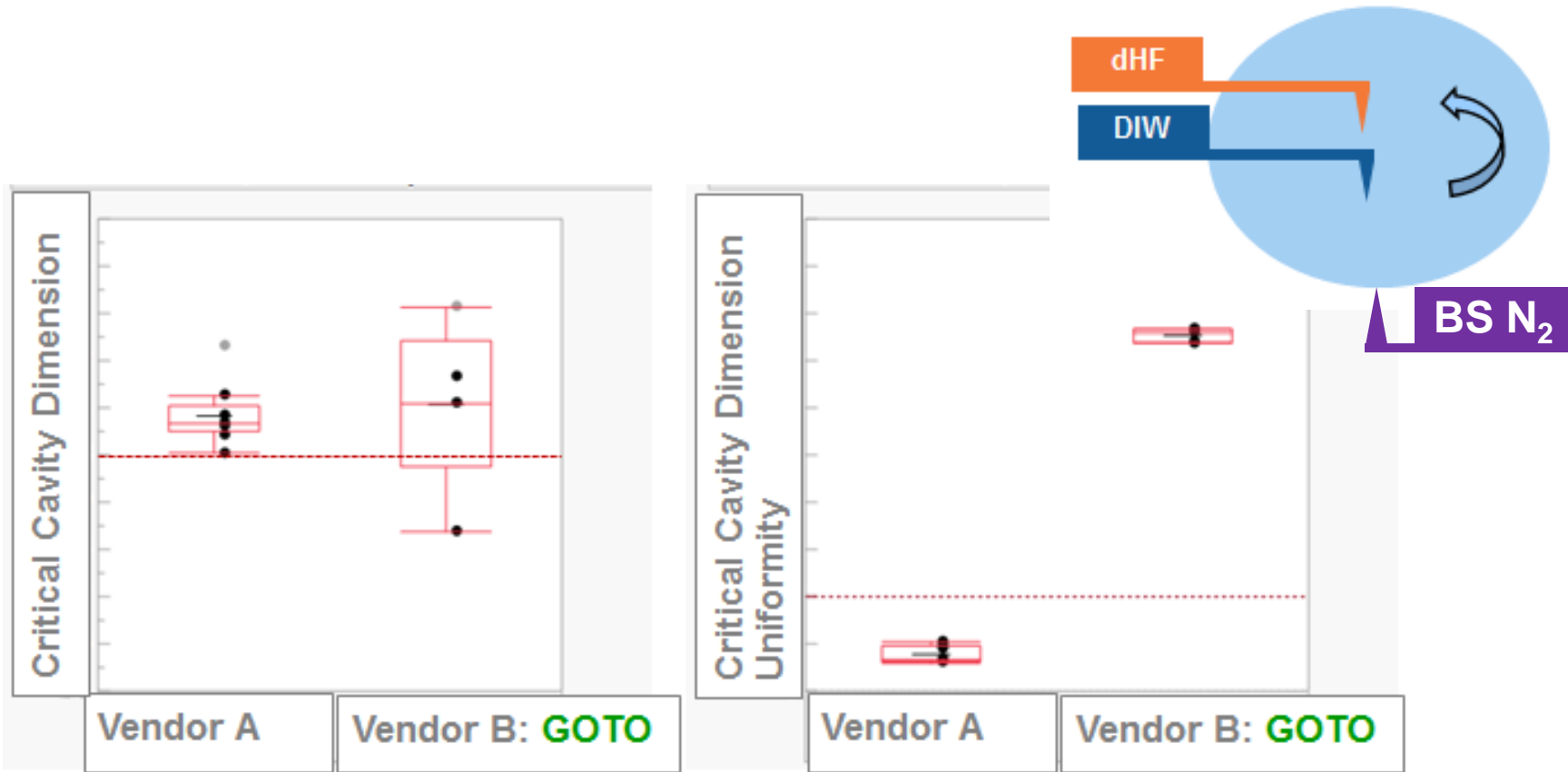
- In sub 1x nm wet cleans, the pre-epi wet clean requires complete post etch residue removal and precise partial removal of SPCR Ox while leaving the rest of the exposed oxide and other materials intact



- Pre-epi wet clean step done with dHF /IPA drying on single wafer clean SNK does not meet cavity size WIW uniformity process specifications

- Hence, a decision was made to transfer this critical clean step to a different wet clean vendor toolset, from Vendor A to Vendor B

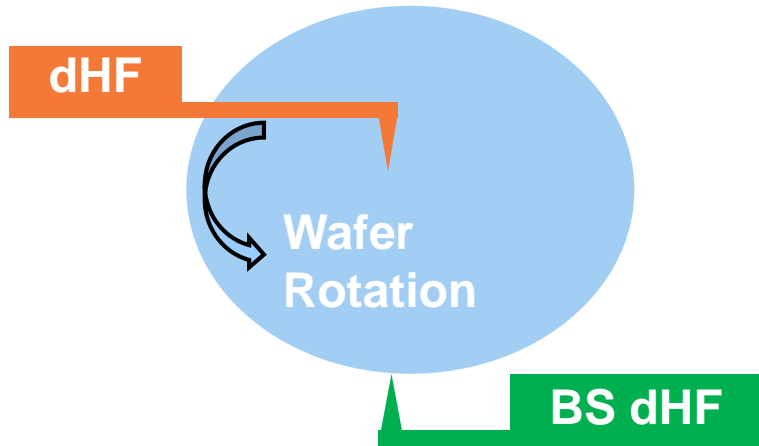
# Improving WiW Uniformity: Adding BS N<sub>2</sub>



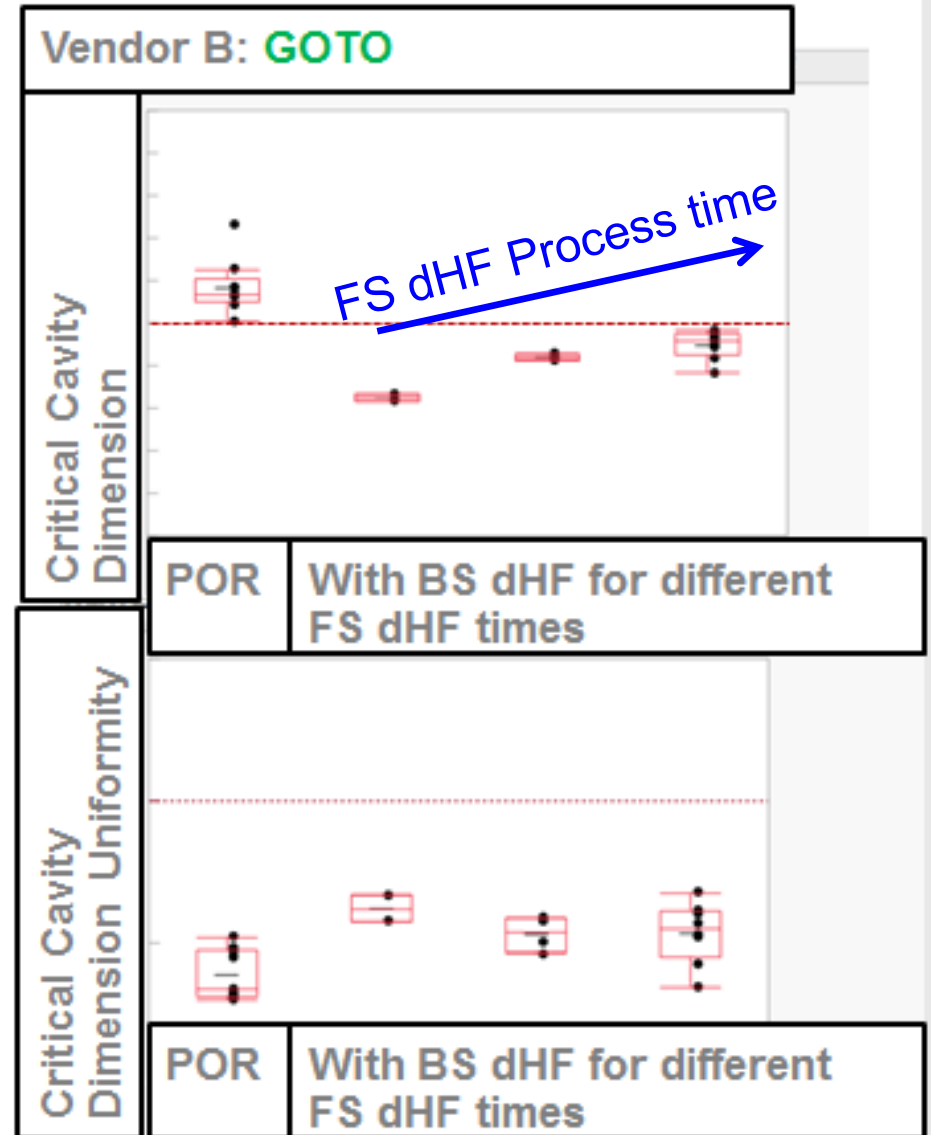
❑ Adding N<sub>2</sub> to wafer backside in vendor B tool gave worse performance

👉 Need to change process/ hardware/ software settings in GO TO tool to ↓ WiW non-uniformity

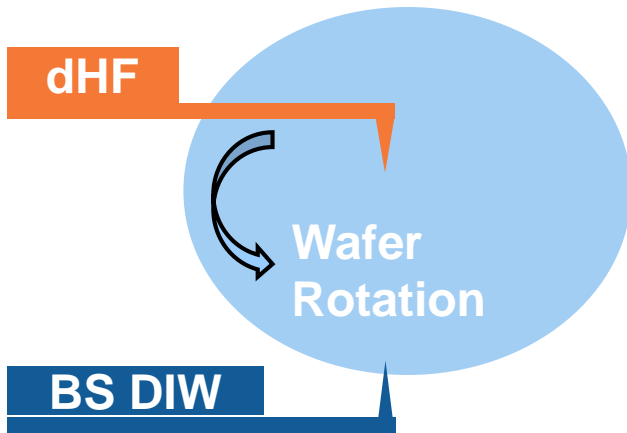
# Improving WiW Uniformity: Adding dHF on Wafer BS



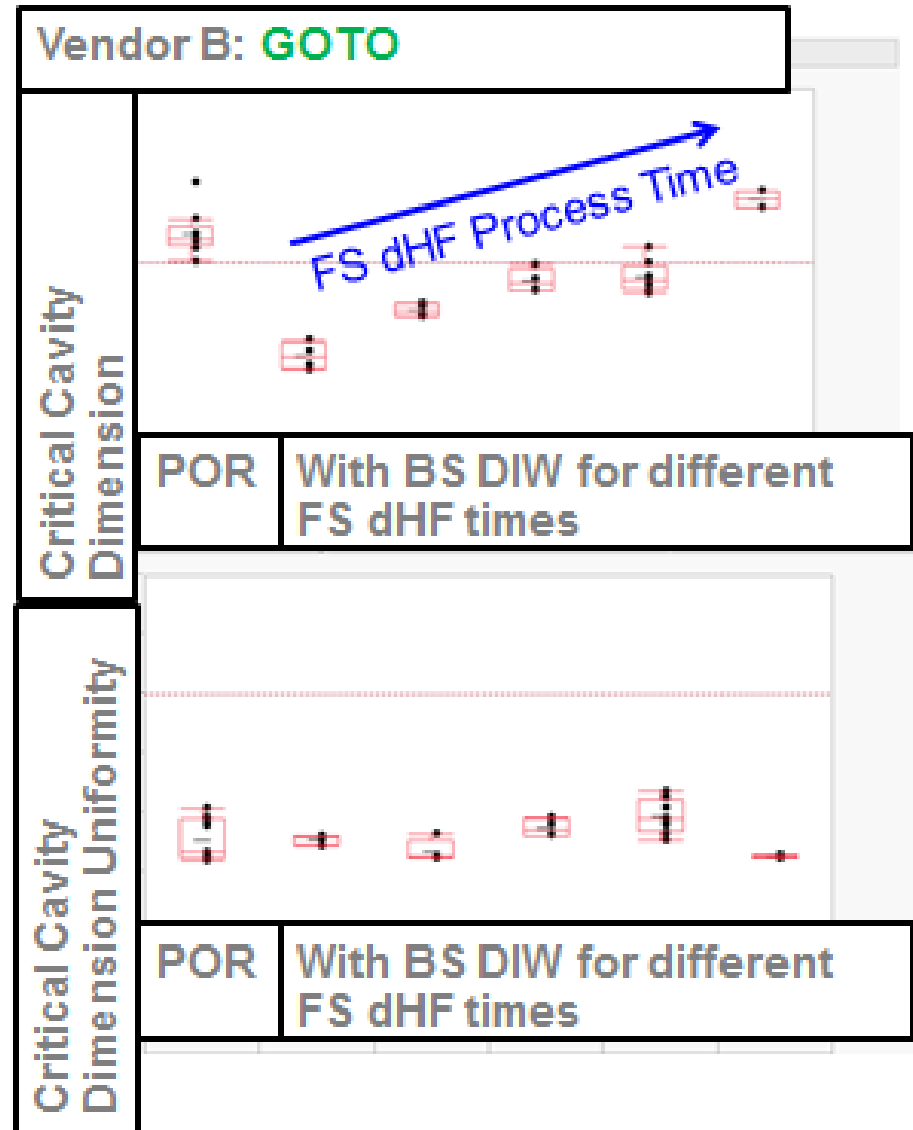
- Had to increase FS dHF time to match removal in Vendor A tool
- Generating many BS particles with dHF only on wafer BS*



# Improving WiW Uniformity: Adding DIW on Wafer BS



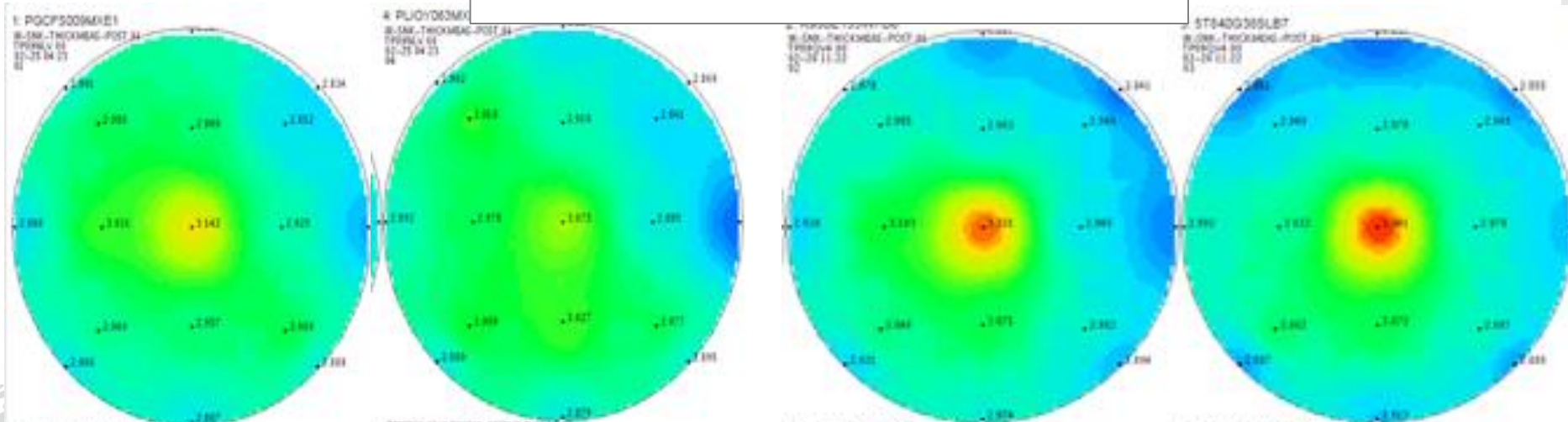
- With FS dHF and BS DIW process, only process time needs to be dialed in to achieve target critical cavity dimension



# Improving WiW Uniformity: Effect of Flow on Wafer BS

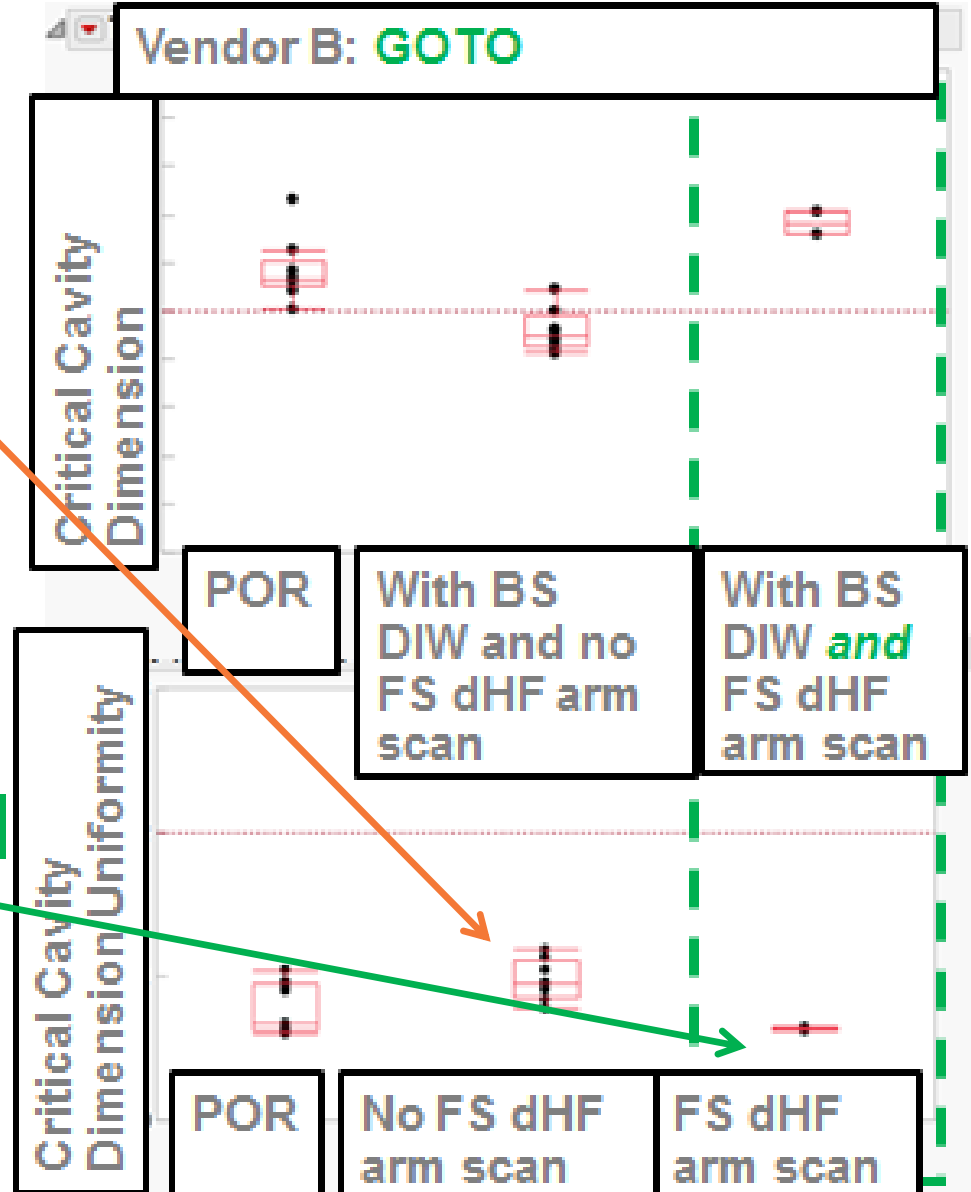
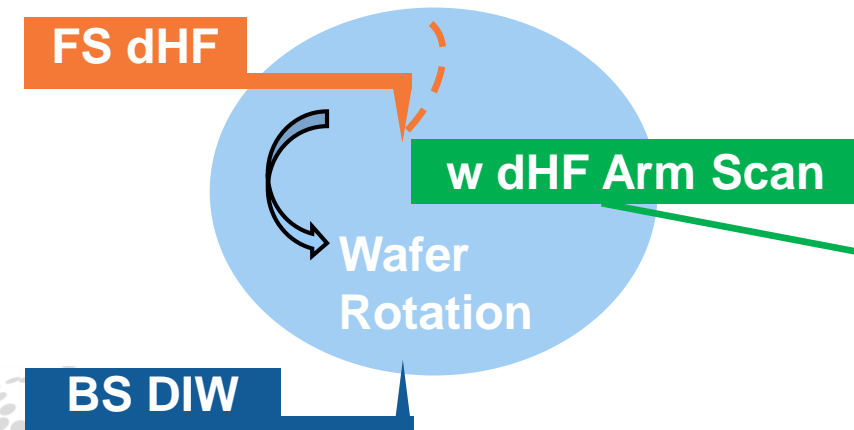
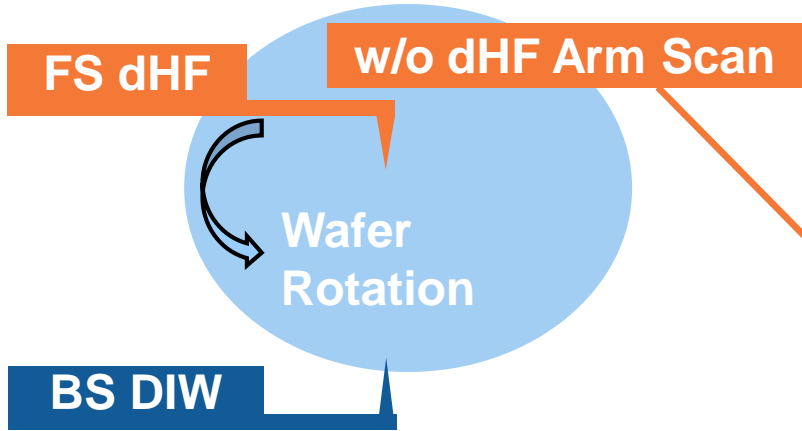


Blanket OX Test Wafer Data Shown

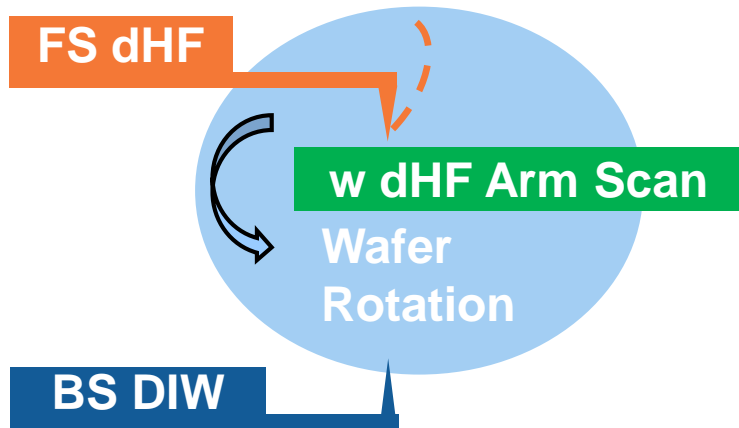


BS dHF is generating excessive removal on wafer FS!

# Improving WiW Uniformity: Adding DIW on Wafer BS + FS dHF scan



# Final HVM Setting on Vendor B Tool



## HVM LEARNINGS:

- ❑ Need to change process time to match critical cavity dimension achieved on Vendor A tool
- ❑ Adding BS flow makes WiW temperature uniform on wafer FS
- ❑ For wafer BS, recommend using DIW, than dHF, to prevent BS particle generation and center removal signature
- ❑ Need chemical dispense arm scan to minimize WiW non-uniformity



# Summary

- ❑ DIO<sub>3</sub> based clean with upstream etch process changes gave the lowest C, O and F contamination levels on the XPS pad but does not reflect reality
- ❑ Developed a **new pre-epi wet clean** that:
  - ❑ ↓ R<sub>on</sub> (same measured for not shown transistor metrics such as DIBL, I<sub>eff</sub> etc.)
  - ❑ Cavity size is unchanged
  - ❑ ~ 50x ↓ in missing epi defects
  - ❑ **Further optimization is in progress**
- ❑ To meet cavity size WiW uniformity requirements, had to transfer wet clean process to new vendor SNK
  - ❑ Adding BS flow makes WiW temperature uniform on wafer FS
  - ❑ For wafer BS, recommend using DIW, than dHF, to prevent BS particle generation and center removal signature
  - ❑ Need chemical dispense arm scan to minimize WiW non-uniformity

# Acknowledgements

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- ❑ Wet Cleans, Metrology and Defect Inspection
- ❑ Integration, Device and, TCAD



# Thank You



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