Cleaning Trends for Advanced Nodes

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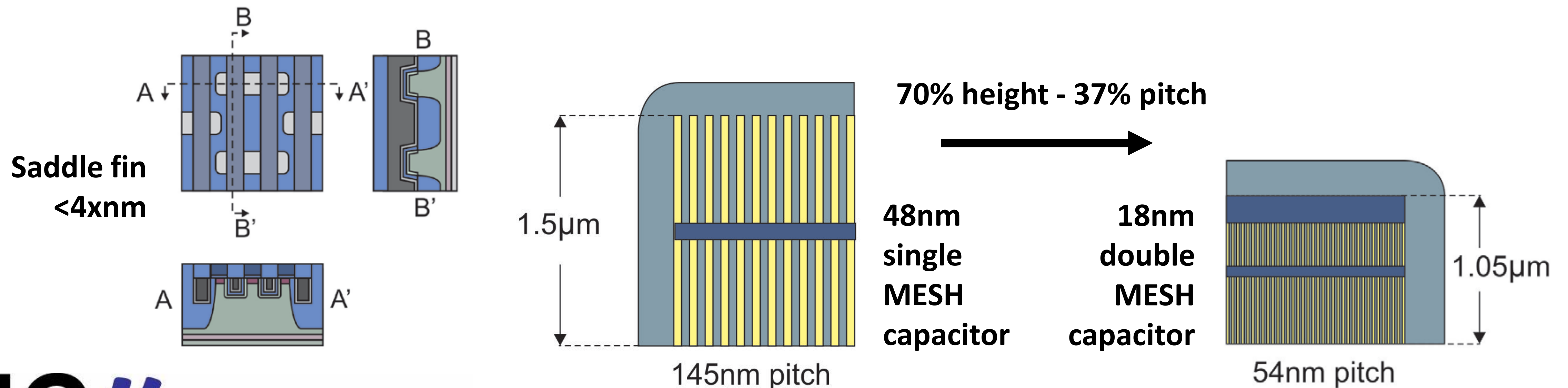
Outline

- DRAM
- Logic
- NAND
- Conclusion

DRAM Nodes

	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Micron	31		25	20			16		14	
Samsung		26		20		18		15		12
SK Hynix		30	26		21	18			14	

DRAM nodes are defined as the smallest half-pitch on the device, Word Line for Micron and Active for Samsung and SK Hynix.



DRAM Scaling Issues

- DRAM capacitors are fabricated at the limits of mechanical stability (see figure on the right). A titanium nitride storage node is formed and then the dielectric layer and top plate are deposited over it.
- Higher K value dielectrics have lower band gaps and therefore higher leakage.
- DRAM scaling has become an optimization battle between achieving a minimum capacitance value, minimizing leakage and optimizing the peripheral circuitry.

$$C = \frac{k\varepsilon A}{t_d}$$ **Capacitance Formula**

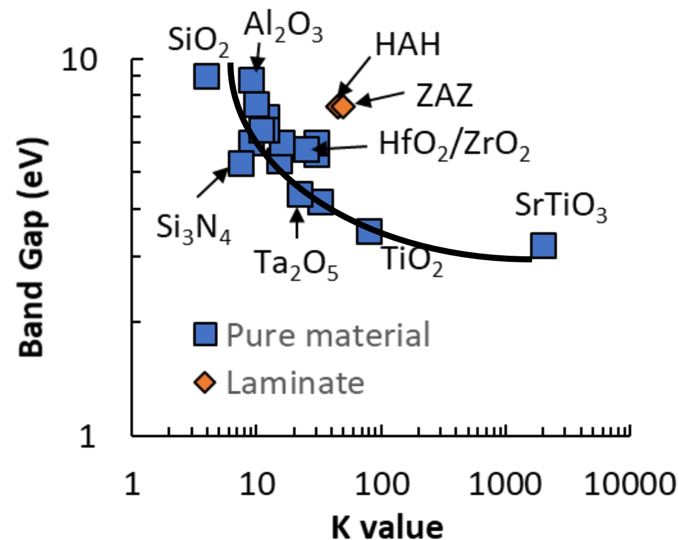
$k = dielectric\ constant$

$\varepsilon = permitivity$

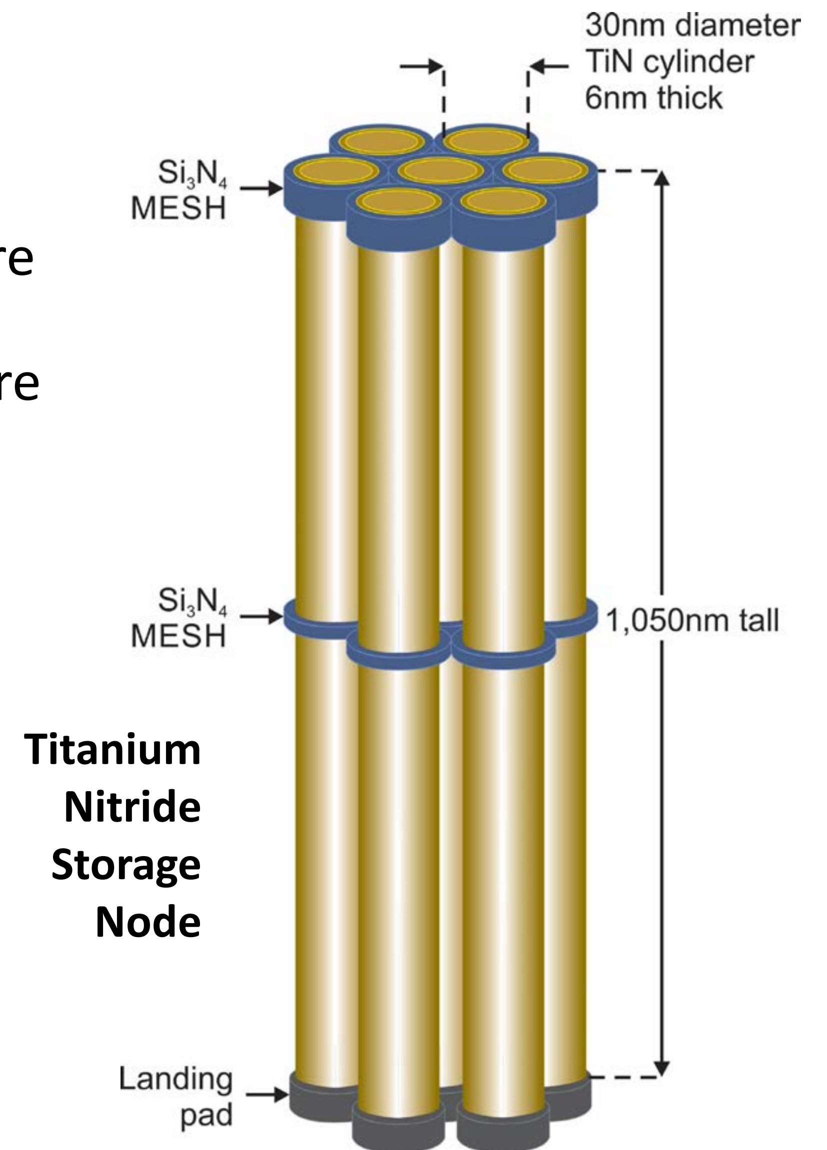
A = area

t_d=dielectric thickness

Band Gap Versus K



Titanium Nitride Storage Node



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DRAM Cleans and Wet Strips - 1

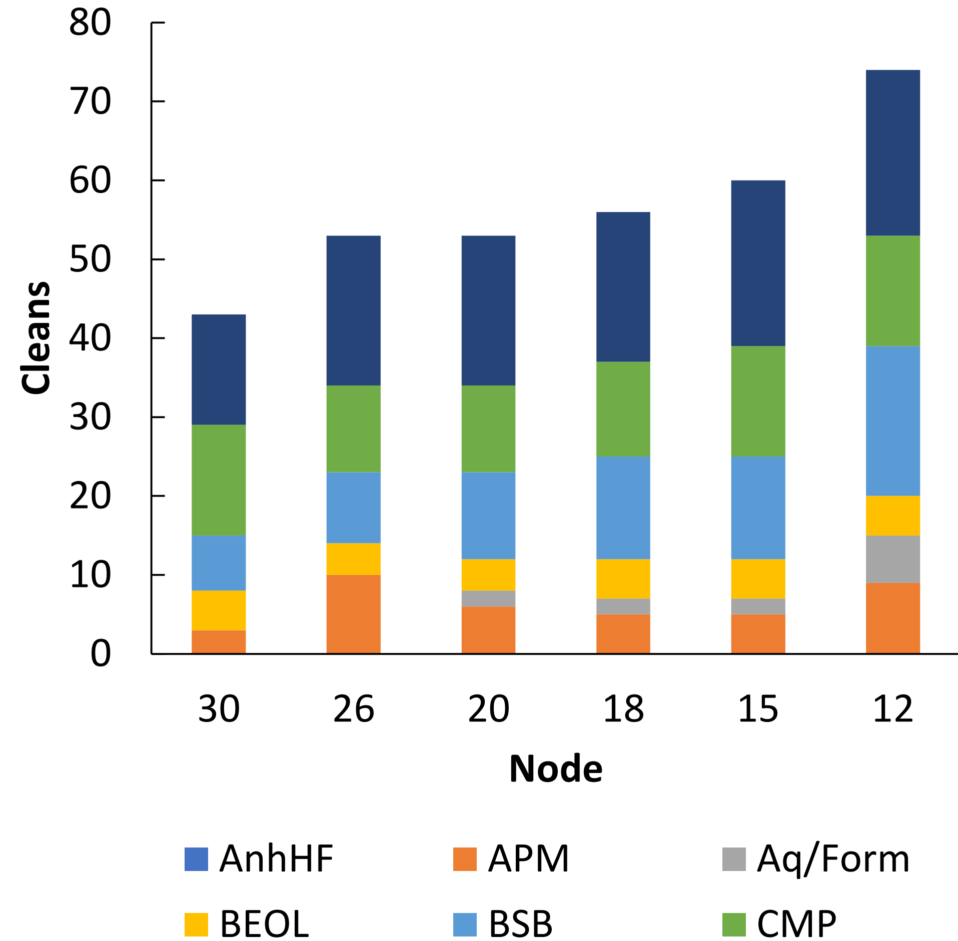
Blocks	Cleans and wet strips
Active	Critical clean, oxide CMP clean
Wells/Thresholds	Ashing and SPM resist strips, critical clean for anneal
Saddle Fin	4 critical cleans, pre pad ox, pre gate ox and 2 pre implant anneals. Tungsten and oxide CMP cleans and wet oxide and nitride strips.
Array protect	Pre pad oxide critical clean
Gate oxides	Pre gate oxide critical cleans, wet oxide etch after thick gate oxide growth
BL Contact	Pre SiGe dep critical clean, SiGe CMP clean
BL/Gate	Wet oxide etch
Extension/Halos	Ashing and SPM resist strips, critical clean for anneal
Spacer	Critical clean
Source/Drains	Ashing and SPM resist strips, critical clean for anneal
Peripheral ESL	Critical clean

DRAM Cleans and Wet Strips - 2

Blocks	Cleans and wet strips
Si Memory Post	Critical clean
PMD	PMD = pre metal dielectric. Post oxide CMP clean
FEOL multi pattern	Multiple APM cleans in each multipattern usage
M1	Critical clean for silicide formation, possible anhydrous HF. Wet cobalt strip, wet oxide etch. Post tungsten CMP clean.
PMD/ILD1	ILD = interlevel dielectric. Post oxide CMP clean
Storage Node	Nitride and oxide wet etches. Wet photoresist strip. Post oxide CMP clean
ILD1	Post oxide CMP clean
BEOL	Post via etch cleans, post aluminum etch cleans, damascene/dual damascene copper CMP clean (one for each layer), tungsten CMP cleans.
BEOL Multipattern	Multiple semi aqueous/formulated cleans in each multipattern usage
BSB	Backside bevel clean for each ArFi exposures FEOL and BEOL

DRAM Cleaning Counts

- DRAM Cleaning Count Trend.
- These cleaning counts are based on a Samsung DRAM process.
- Clean types
  - AnHF – anhydrous HF
  - APM – ammonium-peroxide
  - Aq/Form – semi aqueous/formulated for multi-patterning
  - BEOL – post metal or via etch
  - BSB – backside bevel for immersion lithography
  - CMP – post CMP clean
  - Crit – full RCA style clean



DRAM Cleaning Counts [1]

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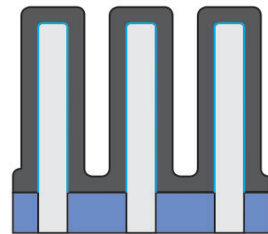
[1] IC Knowledge – Strategic Cost Model – 2018 – revision 01

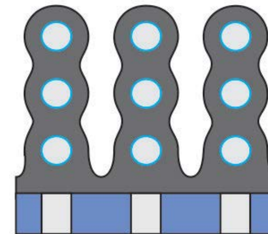
Logic Nodes

	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
GLOBALFOUNDRIES		28			14FF			7FF		5?
Intel [1]	22FF			14FF			10FF			7FF
Samsung	28		20	14FF			10FF	7FF	6/5FF	4HNS
TSMC	28			20	16FF		10FF	7FF	5FF	

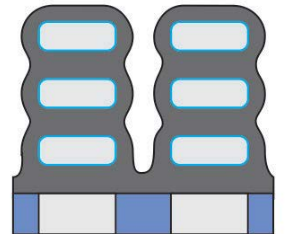
[1] Intel nodes are roughly equivalent to the next smaller foundry node, e.g. Intel 10nm ~ foundry 7nm.



FinFET (FF)



Nanowire (HNW)



Nanosheet (HNS)

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Logic Technology Transitions

Intel/ Foundry nodes	New technology and impact on cleans and wet strips
90/65	Embedded SiGe (eSiGe), critical clean
45/28	High-K Metal Gate (HKMG), replacement metal gate requires sacrificial poly and then replacement gate, critical cleans and CMP cleans.
22/14	FinFET, multiple STIs in some case with critical cleans and CMP cleans, raised NMOS drain, critical clean.
10/7	Multiple work functions to set threshold voltages. Eliminates threshold implants and threshold masks that required ashing/SPM strips. Cobalt filled contacts or local interconnects, cobalt CMP cleans.
5/3	Stacked nanowire/nanosheets, selective SiGe removal and cleaning into cavities. Ruthenium cleans?

Logic Cleans and Wet Strips - 1

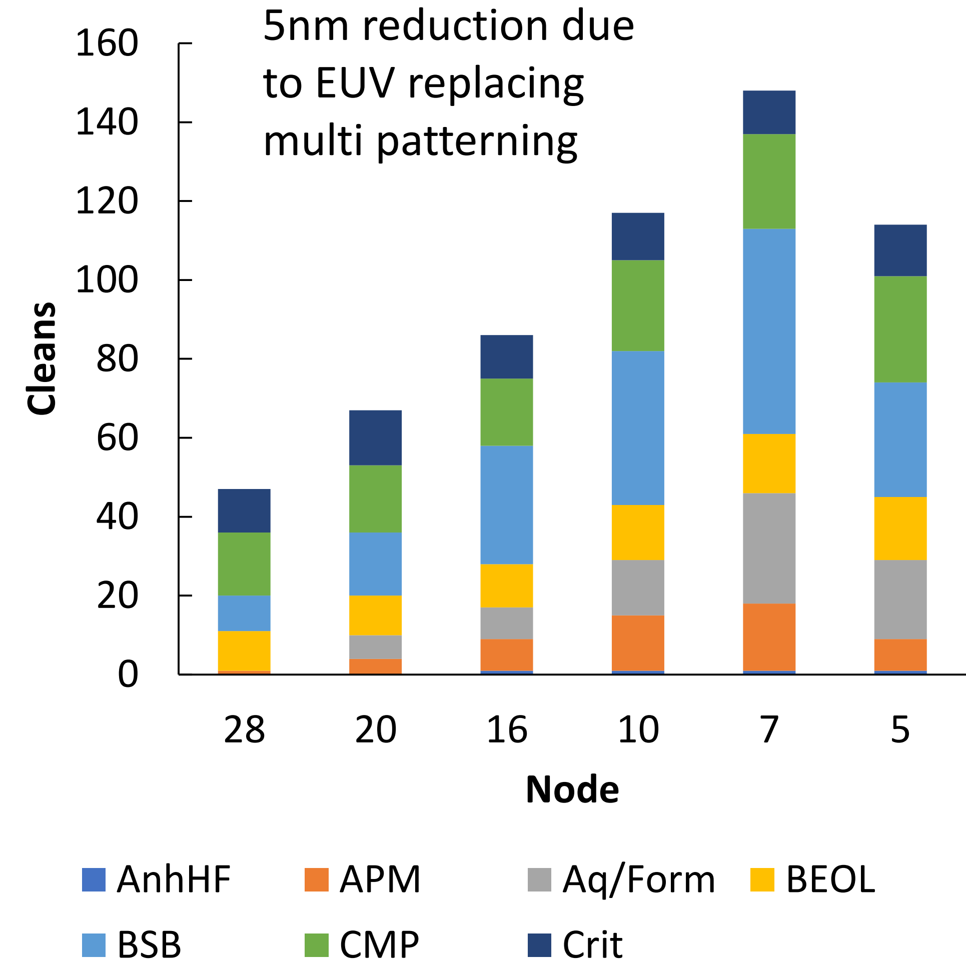
Planar Blocks	FinFET Blocks	Cleans and wet strips
STI	STI(1-3x)/Fin	Critical clean, anhydrous HF <45nm for fins, oxide CMP clean. FinFET processes have 1 to 3 STIs that each require a set of cleans.
Wells/Thresholds	Wells	Ashing and SPM resist strips, critical clean for anneal
Dummy Gate	Dummy Gate	Critical clean for gate dep and for poly ox (2 cleans), poly CMP clean
Extension/Halo	Thresholds	Ashing and SPM resist strips, critical clean for anneal
Spacer	Spacer	Critical clean
Raised S/Ds	Raised S/Ds	Critical clean (one for each), anhydrous HF <45nm
Source/Drains	Source/Drains	Ashing and SPM resist strips, critical clean for anneal
FEOL Multipattern	FEOL Multipattern	Multiple APM cleans in each multipattern usage
Silicide	Silicide	Critical clean, anhydrous HF <45nm
Dual Gate Oxide	Dual Gate Oxide	Critical clean (DGO is an option within RMG)

Logic Cleans and Wet Strips - 2

Planar Blocks	FinFET Blocks	Cleans and wet strips
Replacement Metal Gate	Replacement Metal Gate	Gate open CMP clean, wet sacrificial poly strip, critical clean, second wet sacrificial poly strip, work function metal CMP clean
Contacts	Contacts	SC1 cleans (one for each) , contact fill CMP clean (one for each)
BEOL	BEOL	Post via etch cleans, post aluminum etch cleans, damascene/dual damascene copper CMP clean (one for each layer)
BEOL Multipattern	BEOL Multipattern	Multiple semi aqueous/formulated cleans in each multipattern usage
BSB	BSB	Backside bevel clean for each ArFi exposure FEOL and BEOL

Logic Cleaning Counts

- Logic Cleaning Count Trend.
- These cleaning counts are based on a TSMC process.
- Clean types
  - AnHF – anhydrous HF
  - APM – ammonium-peroxide
  - Aq/Form – semi aqueous/formulated for multi-patterning
  - BEOL – post metal or via etch
  - BSB – backside bevel for immersion lithography
  - CMP – post CMP clean
  - Crit – full RCA style clean



Logic Cleaning Counts [1]

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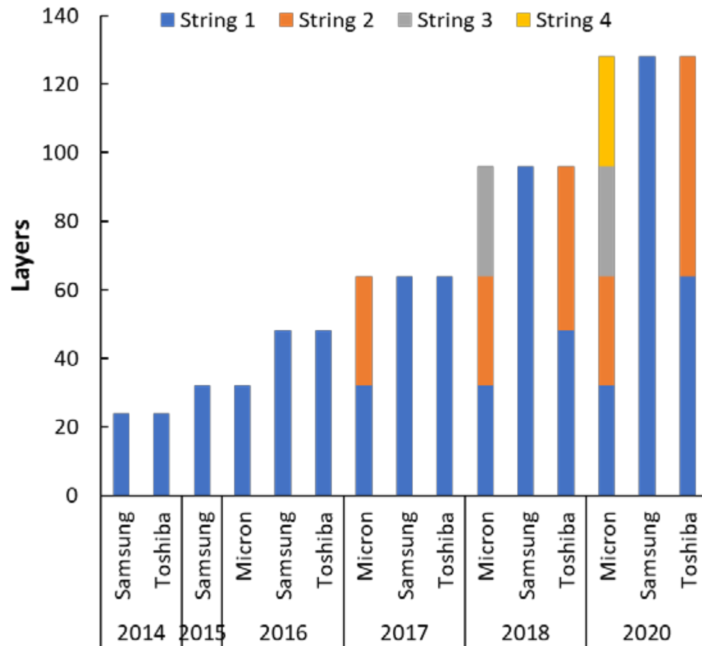
[1] IC Knowledge – Strategic Cost Model – 2018 – revision 01

3D NAND Fabrication

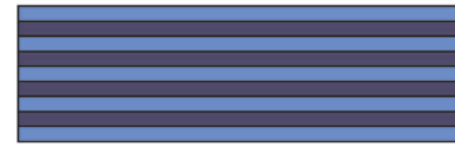
1. CMOS fabrication – some of the CMOS may be under the array – requires interconnect under the array.
2. Memory array formation – single string or string stacking. String stacking repeats layer deposition and channel hole etch with single channel hole fill.
3. Interconnect



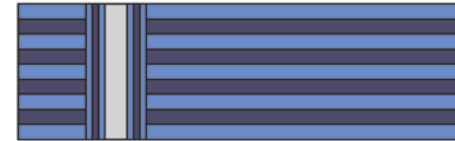
Layers and strings

Memory array masks

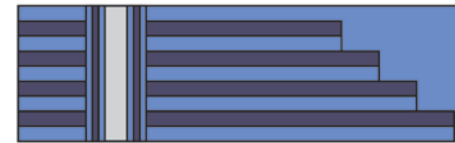
- Channel mask
- 1 stair step mask for each 8 to 10 layers
- 1 or 2 slot masks
- Via mask
- Clear out masks



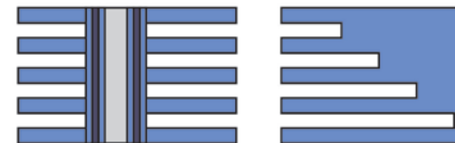
- Deposit alternating layers of SiO and SiN.



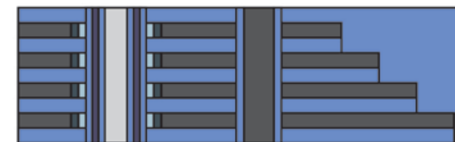
- Mask and etch channel hole.
- Deposit SiO-SiN-SiO (ONO).
- Fill with pSi.



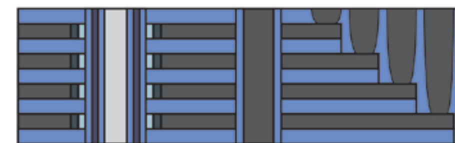
- Stair step mask and etch. A series of partial etches and photoresist trims are done.



- Mask and etch slot.
- Strip out SiN.



- Deposit AlO, TiN, W.
- Etch back.
- Deposit SiO.
- Fill with W



- Mask and etch vias.
- Fill with W

Memory array string formation (Samsung/Toshiba)

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3D NAND Cleans and Wet Strips - 1

Blocks	Cleans and wet strips
Active	Critical clean and oxide CMP clean
Wells/Thresholds	Ashing and SPM resist strips, critical clean for anneal
Gate oxides	Pre gate oxide critical cleans, wet oxide etch after thick gate oxide growth
Gate	Critical clean
Extension/Halos	Ashing and SPM resist strips, critical clean for anneal
Spacer	Critical clean
Source/Drains	Ashing and SPM resist strips, critical clean for anneal
Memory Layers	Critical clean
Channel	4x critical cleans, pre Epi, pre poly dep, pre poly oxide growth and pre poly plug dep. Post oxide and poly CMP cleans
Stair Step	Post oxide CMP for all stair steps except the first one

3D NAND Cleans and Wet Strips - 1

Blocks	Cleans and wet strips
Slot	3x critical cleans, pre gate oxide, pre liner dep, pre TiN dep. Post W CMP clean. Wet sacrificial nitride removal
BEOL	Post via etch cleans, post aluminum etch cleans, damascene/dual damascene copper CMP clean (one for each layer)
BEOL Multipattern	Multiple semi aqueous/formulated cleans in each multipattern usage
BSB	Backside bevel clean for each ArFi exposure FEOL and BEOL

3D NAND Cleaning Counts

- 3D NAND Cleaning Count Trend.
- These cleaning counts are based on a Samsung process.
- Clean types
  - AnHF – anhydrous HF
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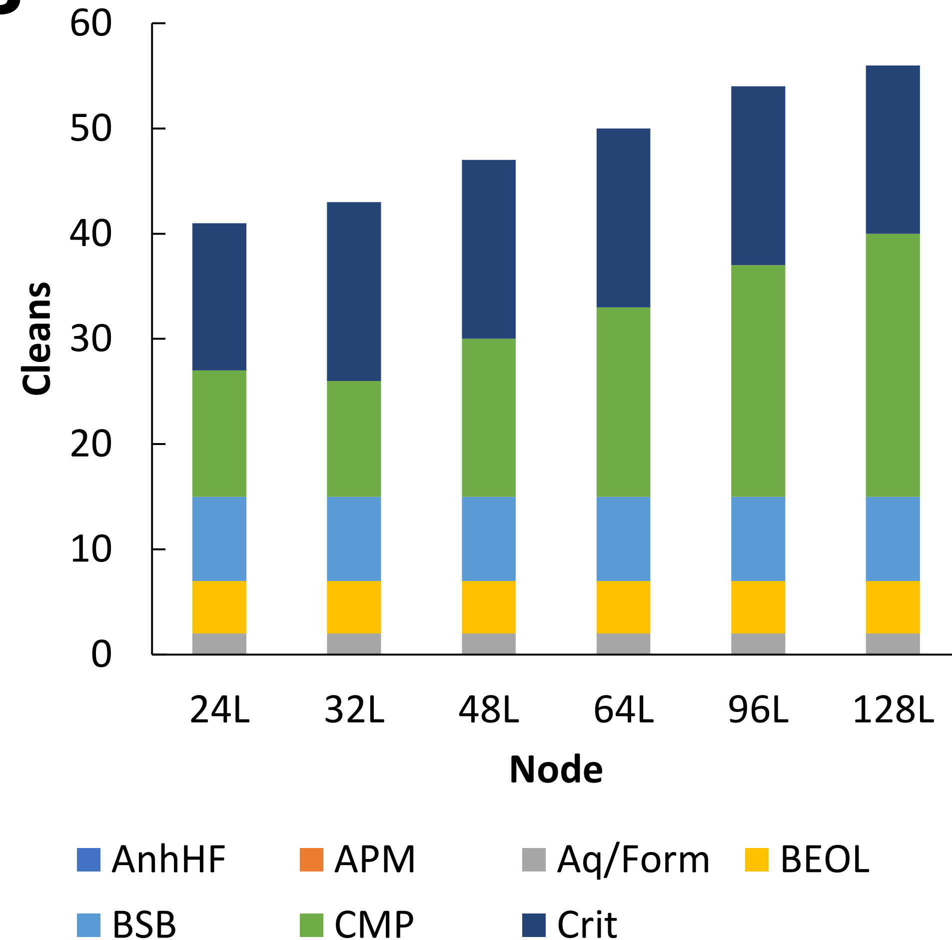

3D NAND Cleaning Counts [1]

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[1] IC Knowledge – Strategic Cost Model – 2018 – revision 01

Conclusion

- DRAM scaling is facing fundamental physical issues with no clear solution in sight.
- DRAM cleans are growing driven mainly by multi-patterning and more immersion lithography layers.
- Logic continues to scale with 5nm and 3nm nodes on the horizon. Nanowires and nanosheets will present new cleaning challenges.
- Logic cleans are growing rapidly mainly driven by multi-patterning and growing mask layer counts, but at 5nm EUV has the potential to significantly reduce the number of lithography related cleans.
- NAND scaling has switched to 3D layer based scaling with a path into at least the middle of the next decade.
- 3D NAND cleans are growing driven by CMP cleans related to stair step formation.