Design Technology Co-Optimization Approaches for Integration and Migration to CFET and 3D Logic

SPCC 2019 Conference

Jeffrey Smith

TEL Technology Center America LLC, Albany NY
Has Dennard scaling has reached its limits?

ITRS Roadmap ref. R. Courtland. IEEE Spectrum
Much of scaling progression over last several nodes has been through DTCO

<table>
<thead>
<tr>
<th>Module</th>
<th>Challenge</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEOL</td>
<td>Interconnect resistance / intra-cell routing resistance</td>
</tr>
<tr>
<td>FEOL</td>
<td>FET capacitance</td>
</tr>
<tr>
<td>BEOL</td>
<td>Power distribution and rail resistance</td>
</tr>
<tr>
<td>MOL</td>
<td>Contact resistance</td>
</tr>
<tr>
<td>FEOL</td>
<td>Transistor performance without increasing power</td>
</tr>
<tr>
<td>BEOL</td>
<td>Via resistance</td>
</tr>
<tr>
<td>MOL</td>
<td>Self-alignment of VCT / VCG with no shorting</td>
</tr>
<tr>
<td>FEOL</td>
<td>Single FIN variation control</td>
</tr>
<tr>
<td>FEOL</td>
<td>P/N Junction scaling for FINFET / Nanosheet</td>
</tr>
<tr>
<td>FEOL / BEOL</td>
<td>CPP / Mx scaling progression / TDDB</td>
</tr>
<tr>
<td>MOL</td>
<td>Wrap-around contact for FINFET / Nanosheet</td>
</tr>
</tbody>
</table>

6T with 3CD power rail + SAGC / SDB boosters

5T with buried power rail + FSAV

<5T CFET buried power rail + FSAV

45nm CPP / 21nm Mx / 16nm wide LNS

AOI standard cell
Single FIN processing key to this scaling – cleans technology has enabled

- More densely packed FINs
- Removal of individual FINs in FIN-cut-last approach
- No significant gouging into bulk silicon for FIN stability
- Single SSD film for FIN doping / selective removal of SSD films in FIN doping process
Focus of DTCO concepts have been to reduce cell size independent of $L_g$

- **Benefits of Self-Aligned Gate Contact (SAGC)**
  - No dedicated tracks for gate contacts \((\text{area})\)
  - Elimination of M0G results in reduction in number of dummy gates \((\text{area})\)
  - Via-to-gate and via-to-S/D sizes can be widened to provide resistance improvement \((\text{power})\)
  - Larger vias drive EUV throughput improvements \((\text{cost})\)
DTCO concepts can also focus on power and performance improvements.

SAGC using 18nm VG / VD

MOL resistance 50.6 Ω

SAGC using 26nm VG / VD

MOL resistance 31.5 Ω
DTCO concepts provide a number of opportunities for new cleans opportunities

- RG with SiN cap
- Gate spacer deposit
- S/D formation
- SiN cap removal
- RG open
- HKMG deposition
- MG recess
- MG cut last
- MG cut fill with SiN and CMP
- SAC
- CESL liner removal
- Ti deposition on S/D epi
- Ru fill into MD and CMP
- MD metal recess
- TiN liner removal
DTCO concepts provide a number of opportunities for new cleans opportunities

- MD cap deposition
- CMP
- M0 memorization into TiN
- VG transfer to MG cap
- MG cap open
- MG plug with SoC
- VD transfer to MD cap
- M0 trench open
- Ru fill and CMP
- M0 recess for FSAV
- TiN liner removal
Co-optimization of films and etch processes through simulation

<table>
<thead>
<tr>
<th>Films Etched</th>
<th>Selectivity</th>
<th>Min distance VD-MG</th>
</tr>
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<tbody>
<tr>
<td>A : B</td>
<td>10 : 1</td>
<td>10.6 nm</td>
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<td>A : C</td>
<td>4 : 1</td>
<td></td>
</tr>
<tr>
<td>B : A</td>
<td>10 : 1</td>
<td></td>
</tr>
<tr>
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<td>4 : 1</td>
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<td>13.0 nm</td>
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<td>A : C</td>
<td>20 : 1</td>
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<tr>
<td>B : A</td>
<td>5 : 1</td>
<td></td>
</tr>
<tr>
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<td>20 : 1</td>
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<td>A : B</td>
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<td>17.1 nm</td>
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<tr>
<td>A : C</td>
<td>20 : 1</td>
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<tr>
<td>B : A</td>
<td>10 : 1</td>
<td></td>
</tr>
<tr>
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<td></td>
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</table>
On-silicon demonstration of hardware / materials done in conjunction with IMEC

CH$_3$F/O$_2$-BASED Si$_3$N$_4$ PLASMA ETCH

Selectivity increases with increasing the C-concentration

<table>
<thead>
<tr>
<th>SiCN-POR</th>
<th>SiCN-N$^{++}$</th>
<th>SiCN-C$^{++}$</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si$_3$N$_4$: SiCN-POR ~ 8 : 1</td>
<td>Si$_3$N$_4$: SiCN-N$^{++}$ ~ 14 : 1</td>
<td>Si$_3$N$_4$: SiCN-C$^{++}$ &gt;20 : 1</td>
<td>Si$_3$N$_4$: SiC ~ 20 : 1</td>
</tr>
<tr>
<td>Si$_3$N$_4$: SiCO ~ 6 : 1</td>
<td>Si$_3$N$_4$: SiCO &gt; 6 : 1</td>
<td>Si$_3$N$_4$: SiCO ~ 10 : 1</td>
<td>Si$_3$N$_4$: SiCO ~ 10 : 1</td>
</tr>
</tbody>
</table>

Plasma Etch Selectivity Study and Material Screening for Self Aligned Gate Contact
Dunja Radsic (IMEC) / Marc Demand (Tokyo Electron) SPIE Advanced Litho 2019
Reduced number of routing tracks drive need for via / metal self alignment

- Vias outside of checkboard grid are still self-aligned
- Vias at 21nm pitch (EUV-LELE) can be patterned by single slot-contact

Benefits of FSAV
- Via “CD” are defined by “keep” mask as opposed too direct via (area)
- Across-track vias are allowed and will be self-aligned (area)
- Adds significant freedom to cell layouts
- Improved via resistance with larger via size
Current density reduction as critical as via resistance reduction

Dual Damascene

87.5 ohm

Dual Damascene (M1 to M0)

DoD selective deposition FSAV

65.0 ohm

FSAV (M1 to M0)
On-silicon demonstration of hardware / materials done in conjunction with IMEC

**After M1 CMP**
- Create topography with metal recess etching
- Target = 10nm

**M2V1 Etching**
- Via confined in y-direction by M2 HM
- Via-first etch lands selectively on SiCN barrier
- Topography is maintained by selective removal of SiCN

**M2 Fill**
- Min-distance M1-V2 is maintained by topography
- FSAV is formed

ULK open with selectivity to ESL

Yannick Feurprier

Via (left) and Trench (right) transfer through ULK with stop on ESL

Xinghua Sun

HAR via filling by CVD Ru

Kyle Yu
Moving power rails from M0 provides even further potential PPAC improvement.
Moving power rails from M0 provides even further potential PPAC improvement

- **Benefits of buried power rail**
  - M0 can be occupied by routing tracks (*area*)
  - Rail aspect ratio can be increased to improve resistance (*power*)
  - Rail CD can be traded-off to allow for larger LNS width (*performance*)
New integration challenges arise from new standard cell design approaches

- **Tip-to-tip distances become challenging with 4T cell heights**
  - Increase to 4.5T or 5.0T to provide relief for intercell tip-to-tip
  - Confided S/D epi growth for intracell tip-to-tip
  - Some method of self-aligning cuts to the buried rails

- Wider LNS widths can cause M0A to complimentary S/D shorts
- Confined growth needed
- How does reduced S/D volume impact channel stress / performance?
Significant on-silicon hardware / materials demonstrations on-going

Ru fill with small over-burden

HAR trench Ru filling capability

Ru recess within STI trenches

Wet removal of various liners

K. Yu / J. Hotelan (Tokyo Electron)

N. Joy (Tokyo Electron)

K. Pillai (Tokyo Electron)
Complete removal of any conductor between BPR and device is crucial

SiO
SiO liner
Ru
Silicon
TaN liner

J. Hotalen (Tokyo Electron)

K. Pillai (Tokyo Electron)
Power improvements require additional integrations for delivery networks

"Traditional" supplying rails through upper metal layers

Power delivery to buried rails through back side of wafer

Lars Liebmann (Tokyo Electron)

US 2018/0218973
Donald Nelson, Mark Bohr, Patrick Morrow (INTEL)
Progression from FINFET to Gate All Around (GAA)

**Logic Gate All Around (GAA)**

- At 3nm recent imec work suggests that FinFETs are viable but every scaling booster option is required and nanosheets offer more margin.
- Nanowires provide the best electrostatics, FinFETs provide the best drive current, nanosheet width can tune the trade-off.

**Weff**
- Planar (1 side gate) Weff = W
- FinFET Weff (3 side gate) = 2Fh + Fw
- Nanosheet (4 side gate) Weff = 2NSth + 2NSw

![Effective channel width (Weff).](image)

<table>
<thead>
<tr>
<th>Device</th>
<th>nanowire</th>
<th>FinFET</th>
<th>nanosheet</th>
<th>nanosheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>5nm/5nm</td>
<td>7nm/40nm</td>
<td>18nm/5nm</td>
<td>5nm/50nm</td>
</tr>
<tr>
<td>Relative Weff</td>
<td>0.69</td>
<td>1.00</td>
<td>1.06</td>
<td>1.26</td>
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<tr>
<td>Electrostatics</td>
<td>Best</td>
<td>Good</td>
<td>Better</td>
<td>Better</td>
</tr>
</tbody>
</table>

Nanowire, FinFET and nanosheet relative performance

**IC Knowledge LLC**

**Scotten Jones (IC Knowledge) Nikon Lithovision 2019**
Significant FOEL development done on nanosheet enablement

Subhadeep Kal (SPCC 2018)
Push has been for wider nanosheets at tighter vertical pitches.

**FREQUENCY GAIN OVER 5.5T2 FINFET**

Reported at Vdd and at constant power.

- When reported at constant power, frequency saturates quickly with NNS and W.
- For NNS>=4, increasing W has no impact or degrades performance.
- Many NanoSheets have better performance than FinFETs but few reach 3nm node targets.
- To reach 3nm node targets, small geometry space:
  - NNS=3, W=16nm, PNS=12nm.


*M. Garcia Bardon* VLSI 2018
Increasing sheet widths and BPR puts strain on p/n separation
Wider and more densely packed nanosheets provides cleans / etch challenges

- **Challenges**
  - More difficult to get Angstrom-level precision on ALD deposition around >16nm wide sheets with <2nm “window” between sheets
  - More difficult to remove PMOS WFM from NMOS gate with these same “window” dimensions

- **Complimentary FET is a possible solution**
  - Stack NMOS and PMOS devices on top of one another
  - Enable the p/n separation to be vertical – more room for processing
  - Achieve additional scaling improvement
3D scaling is a logical path beyond N3

- Approach → grow while **squeezing** things **tighter**
- Industry unlikely able to extend beyond 20nm FINFET pitch
- EUV + multiple patterning very expensive for manufacturing

Los Angeles = 2D

Tokyo = 3D

- Approach → grow while **building** things **higher**
- **3D logic** evolution is already here (FINFET → Nanowire → CFET / VFET)
- No need to extend beyond SAQP
- Further push-out of EUV?
Multiple advantages with device-on-device CFET stacking

- n/p separation is now vertical
- Staggered upper / lower M0A enables n and p connections to common routing track
- LNS size can be increased while maintaining <5T height
- Standard cell can be completed at M1
Full benefit of CFET also requires transistor-on-transistor stacking

<table>
<thead>
<tr>
<th>Inverter Buffer</th>
<th>active FET</th>
<th>Usage (%)</th>
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<tbody>
<tr>
<td>INV</td>
<td>1</td>
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</tr>
<tr>
<td>INVx2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>BF</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>BFx2</td>
<td>3</td>
<td>7.5</td>
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<tr>
<td>NAND NOR</td>
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<td></td>
</tr>
<tr>
<td>NAND2</td>
<td>2</td>
<td>3</td>
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<tr>
<td>NAND2x2</td>
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<td>NAND3</td>
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<tr>
<td>AND2</td>
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<tr>
<td>AOI OAI</td>
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<td>AOI22</td>
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<tr>
<td>SDFPQ</td>
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<table>
<thead>
<tr>
<th>Width (CCP)</th>
<th>LGAA</th>
<th>sCFET</th>
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<tbody>
<tr>
<td>INV</td>
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<td>FLOP</td>
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Usage weighted widths

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<thead>
<tr>
<th></th>
<th>LGAA</th>
<th>sCFET</th>
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<tbody>
<tr>
<td>12.11</td>
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<tr>
<td>1.00</td>
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</table>

Lars Liebmann (Tokyo Electron)
Significant integration opportunities for CFET enablement

<table>
<thead>
<tr>
<th>Major process challenges</th>
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<tbody>
<tr>
<td>FEOL interconnects vs FEOL thermal budget</td>
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<tr>
<td>WFM engineering and Vt tuning</td>
</tr>
<tr>
<td>Ox gap fill &amp; etch back - critical Height control</td>
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<tr>
<td>Buried Power Rail high AR trenches / metals in FEOL</td>
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<tr>
<td>Device Sub isolation integration</td>
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<tr>
<td>Dummy PC formation</td>
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<tr>
<td>Source Drain selective in situ doped epitaxy</td>
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<td>Inner Spacer formation</td>
</tr>
<tr>
<td>Split Gate</td>
</tr>
<tr>
<td>3D structure metrology</td>
</tr>
</tbody>
</table>

Daniel Chanemougame  (Tokyo Electron)
Other approaches for 3D logic

**Cell Origami**
- **Challenges**
  - high aspect ratio processes
  - selective etch & deposition
  - pin congestion in routing
- **Value**
  - substantial density scaling
  - familiar design flow

**Sequential Gate-on-Gate Stacking**
- **Challenges**
  - thermal budget in process
  - design flow:
    - cell partitioning
    - timing
    - clock tree synthesis
    - routing with MIV
- **Value**
  - wire-length & power reduction

**Vertical Channel Devices**

**Beyond-CMOS Heterogeneous Integration for AI**

**Challenges**
- height sensitive depositions
- complex integration
**Value**
- substantial density, power, performance improvement
- multi-node solution

**Challenges**
- CNFET
- architecture optimized for AI
**Value**
- very substantial performance improvement

---

@ e.g. Prof. Sung Kyu Lim's group, Georgia Institute of Technology
@ e.g. Prof. Andras Moritz’s ‘Skybridge’ group at the University of Massachusetts Amherst
@ e.g. Prof. Max M. Shulaker’s group now at MIT, work originally done at Stanford

Jeffrey Smith / SPCC2019 / 03 April 2019

Lars Liebmann (Tokyo Electron)