Current and Future Wet Etch Challenges - Scaling in the New Era

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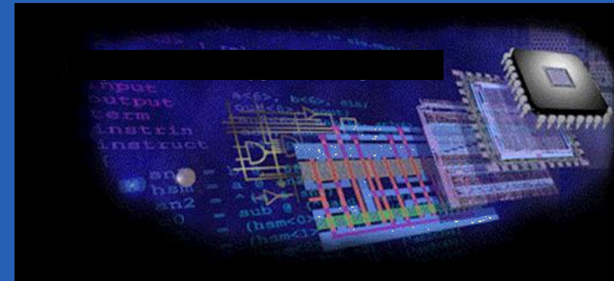
April 1st, 2019

THE SURFACE PREPARATION AND CLEANING CONFERENCE (SPCC)

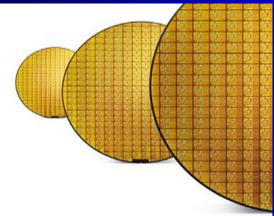
Business of Cleans



Current Technologies

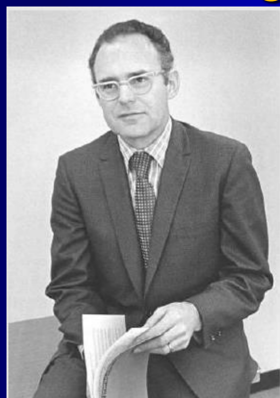
Challenges in 14nm and Above Process Technology Nodes

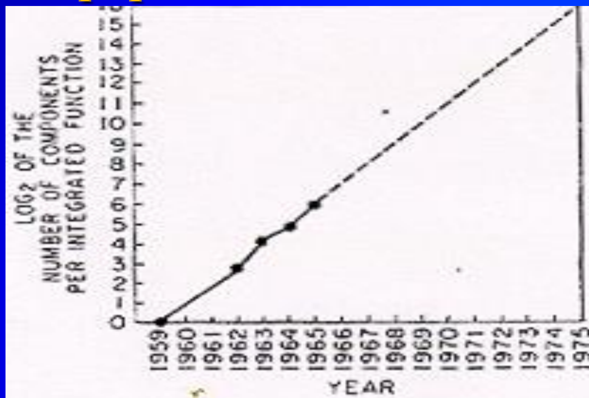
- Moor’s law – Cost Per Transistor and Economics
- Transistor and Interconnects Innovations and Scaling
- Cleans/Wet Etch Requirements & Expectations
- Cost of Contamination and Excursions
- First Line of Defense – Chemical Purity and Filtration
- Beyond 14nm



Moore's Law in Action

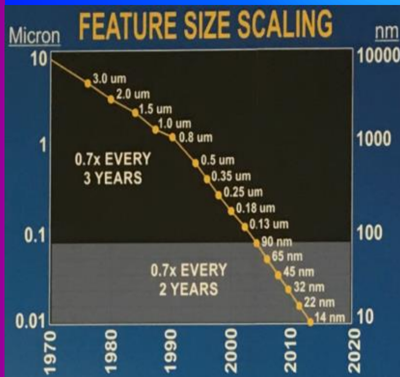
Moore's original paper





Electronics Vol 38, #8 April 19, 1965

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip



Space and Energy Saving Computing

High Performance Computing Power

ASCI Red 1996	Knights Family
1 Tflop 10,000 Pentium Processors 500kW	3 Tflop 72 cores 200W

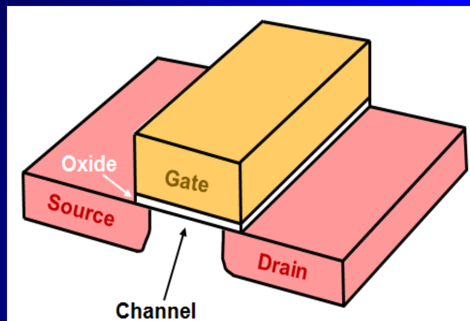
Source: Intel

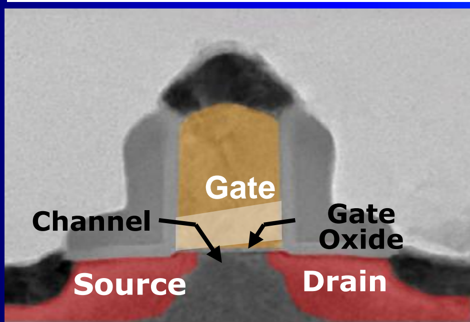
Wet etching/Cleans complexity and demand is continually increasing to Keep up with Moor's law

What dictates FEOL (Transistor) Research Activities?

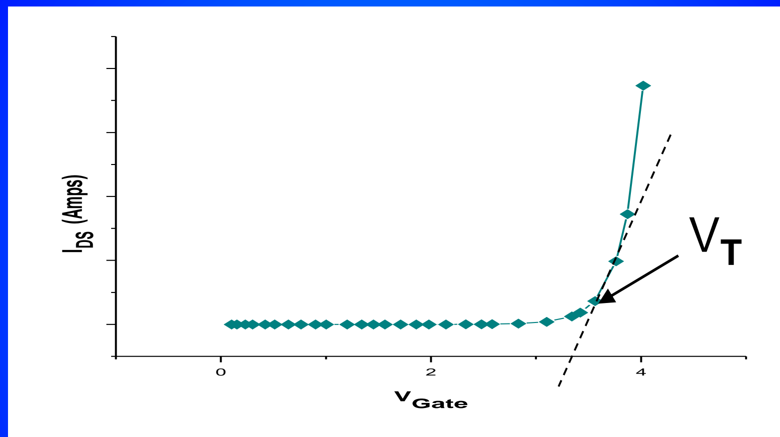
2D

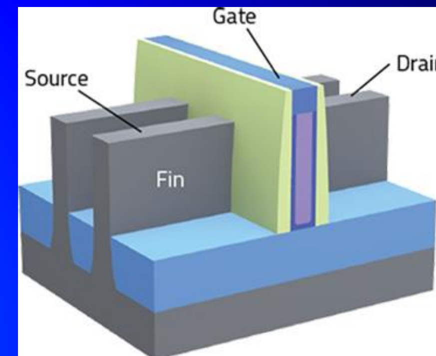
3D



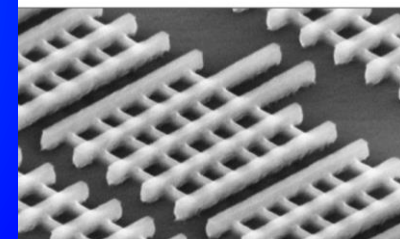


Important transistor parameters





nm Tri-Gate Transistor



$$V_T \propto \frac{1}{C_G} \qquad (V_T - \text{threshold voltage; } C_G - \text{gate capacitance})$$

$$C_G = \frac{\varepsilon_0 \kappa L W}{t} \qquad \begin{pmatrix} \kappa - \text{dielectric constant; } L, W - \text{channel length \& Width} \\ t - \text{gate insulator thickness} \end{pmatrix}$$

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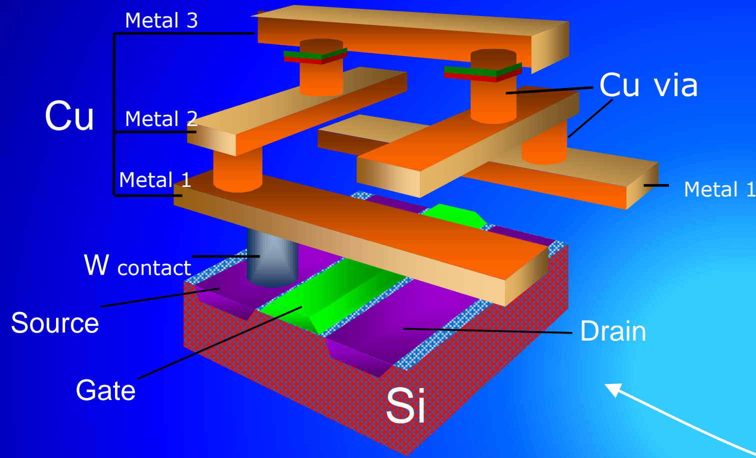
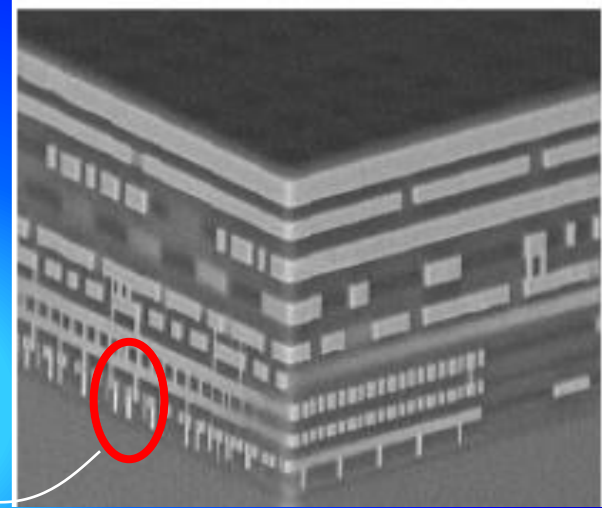
What dictates BEOL (Interconnects) Research Activities?





RC may be reduced by:

$$\tau = RC = (\rho / t_{metal})(\varepsilon / t_d)L^2$$

1. Reducing resistivity ρ (Al→Cu)
2. Increasing metal thickness (t_{metal})
3. Reducing ε (low k dielectrics)
4. Shortening metal line length, L

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Moore's Law Enables Innovation and Cost Reduction

COST PER TRANSISTOR TREND

$ / mm2 (normalized)

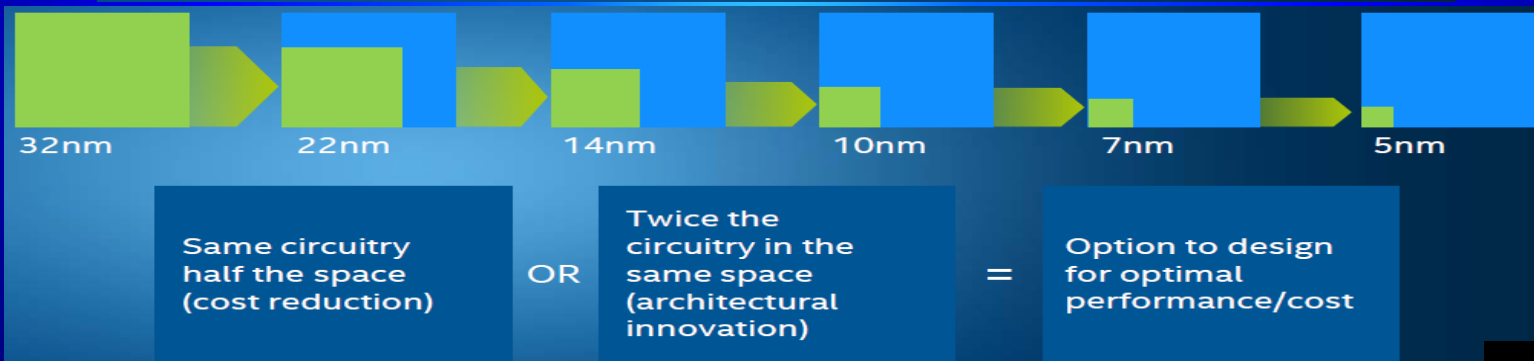
x

mm2 / Transistor (normalized)

=

$ / Transistor (normalized)

130 nm 90 nm 65 nm 45 nm 32 nm 22 nm 14 nm 10 nm 7 nm



Source: Bill Holt, Intel

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Cleans/Wet Etch Requirements & Expectations

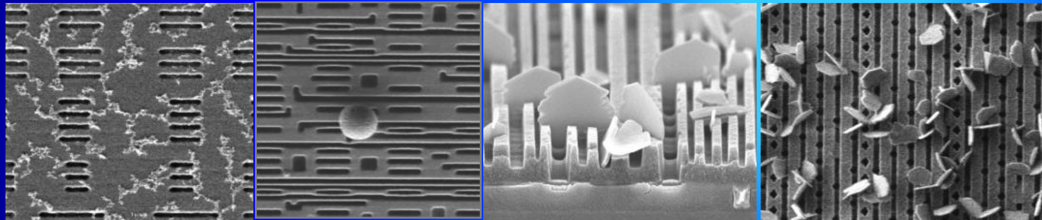
- Increase in cleans steps, chemical demand, and complexity as we march towards smaller dimensions
- Always up and running tools – No interruptions in supply chain → Chemicals/raw materials and equipment spare parts are readily available
- Invest proactively to secure the supply chain → Reduce total cost of ownership
- Effective change control is a key to protecting customers
- Enhance quality and reliability control for clean chemicals
  - Better Etch selectivity →***Etch Selectivity = ER of target material/exposed & underlying material***
  - Eliminate contamination and reduce variability at all levels of supply chain
- Environmentally friendly solutions

Defect reduction, continuous yield improvements and keeping cost per transistor low is the key to the industry's success!!

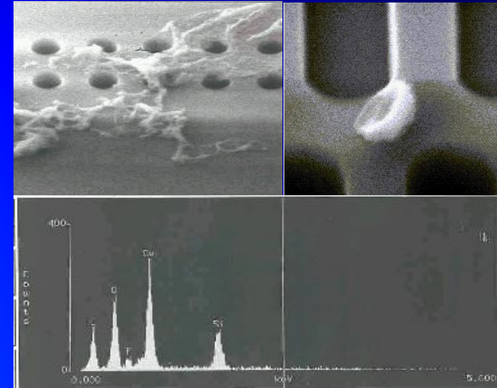
Cost of Contamination/Excursions

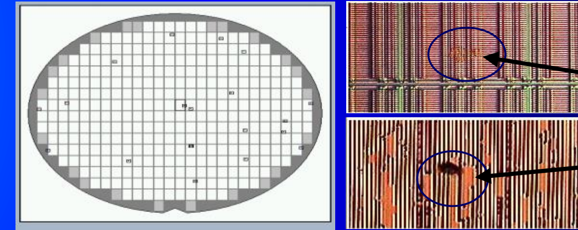
Possible Sources of Particles/Contamination

- Corrosion products → Metal-rich residue
- Electroless deposition of copper Cu^{++} → Cu^{0}
- Precipitation/Nucleation of metallic complexes from the cleaning solution
- Fab environment/facilities
- Etching/Cleaning Chemical components
- Incoming Particles → Chemical supply/raw material
- Zeta potential difference between particle and wafer surface



Source: Nabil Mistkawi, Dissertation





Determining the source/root cause is frequently challenging but extremely important to identify a remedy

- Contaminated raw material effects finished goods quality
- Customers cannot afford excursions: one failure can have a significant financial impact
- Early Detection Lowers Impact to Finished products

First Line of Defense – Chemical Purity

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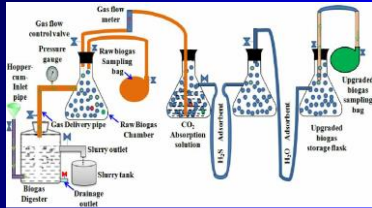
Purification



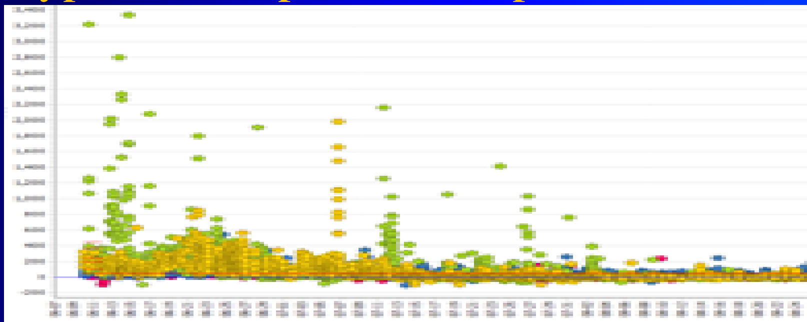
Filtration and Packaging

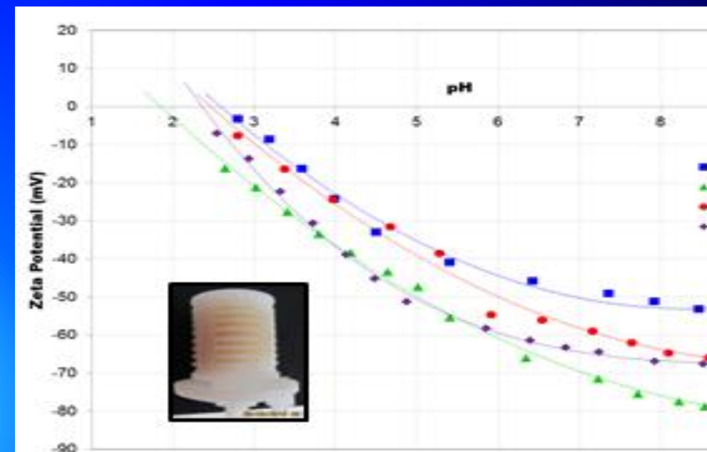
Transportation /Transfer

- Raw material sources, Purification, and filtration are crucial to semiconductor processing.
- Much stricter protocols and further innovations in improving purity and quality control is a key.
- Filters can't introduce contaminants. They must remove and retain impurities without reacting with process chemicals
- It is too late if we wait until a pressure drop is observed → Filter is supersaturated
- Inline and continuous monitoring is vital in catching issues before they occur
- Identifying potential failures and their impact is critical → FMEA
- Collaboration/joint efforts with filter suppliers is needed to drive further improvements.

Product Control and Yield Enhancement via Filtration

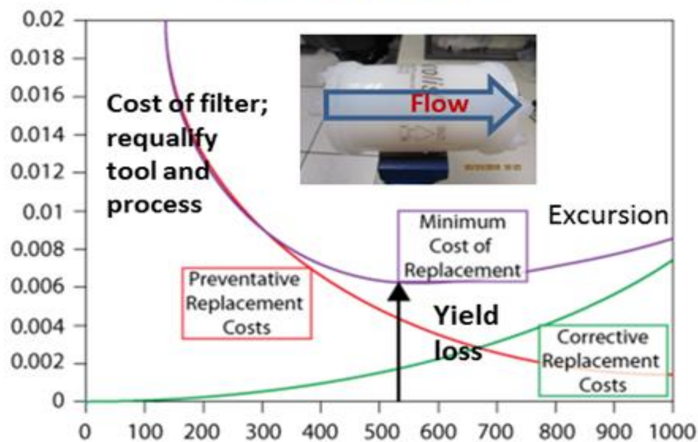
Typical trend post filter replacement





Filter Membrane zeta potential as a function of filter loading

Determining and optimizing the filter cost function



Filtration cost function & performance investigations:

- On wafer evaluations: Surface scans, EDX, TXRF
- Zeta potential studies
- Chemical analysis
- Retention studies
- Filter membrane failure analysis

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Beyond 14nm

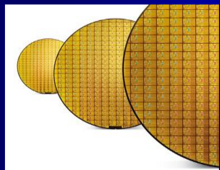
- Non Traditional Scaling – 3D architecture, design innovations, and process sensitivity are increasing
  - Sub 10nm particles are now significant → Enhanced Purity is crucial
  - Filtration Technology must keep up with scaling to meet the paradigm shift in defect tolerance
  - Trace levels of contamination can now have severe impact on yield and device reliability
- Understand particle metrology gap → On blanket wafers vs. in-situ liquid vs. In-line
- Advanced metrology and analytical methods are critical for Defect Identification and Characterization

Decision making will be difficult/flawed without stable and capable metrology

Future Technologies

Challenges for Future Device and Integration Options: 10nm → 3nm technology nodes

- Fin and BEOL ILD lines collapse mitigation -- surface derivatization/modification is required
- Gate pitch scaling → Gate-All-Around (GAA) by fabricating Si, SiGe, and Ge nanowires as transistor channel materials to enable the scaling evolution
- Fin thinning – Ultra Thin Body Transistor (UTBT)
- Potential strategies to mitigate Shot Noise and Line Edge roughness during lithography exposure
- Green chemistries development and the environment --- Outside the box Thinking
- The introduction of new BEOL materials: cobalt, ruthenium, aluminum nitride, etc. mandates further innovations in cleans/wet etching technologies
- Increased mobility fins → III-V elements NMOS, Ge PMOS
- Cleans role to enabling EUV
- Vapor/gas Phase strategies
- 3-D NAND and emerging memory devices --- Wet etch selectivity and vertical uniformity, Pattern collapse, etc.



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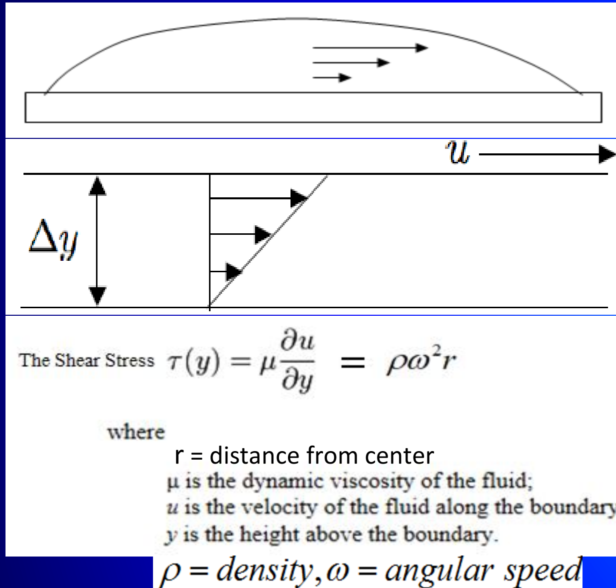
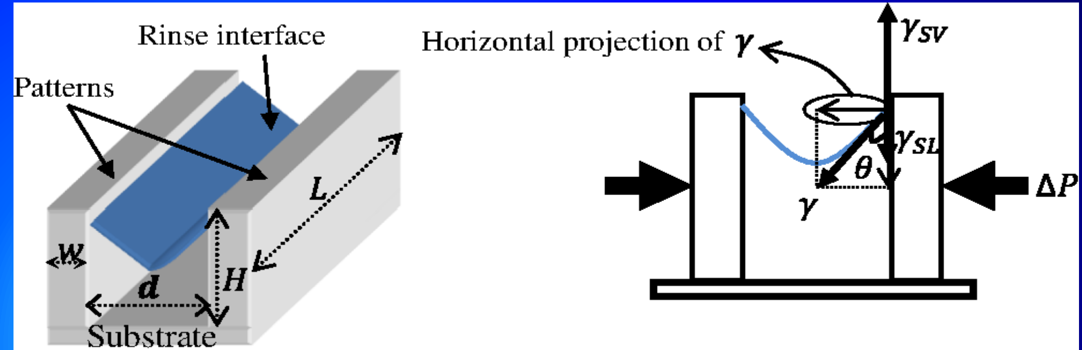
Fin Collapse

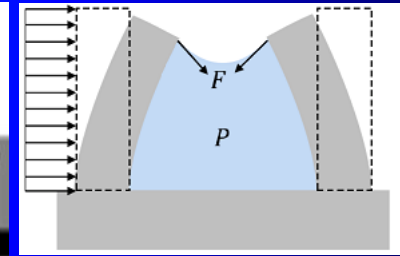
Shear Stress Force



Note the direct relationship between the shear/stress force and density/viscosity

Unbalanced Capillary forces During the drying step





The max stress is described according to:

$$\sigma = \frac{6 \cdot \gamma \cdot \cos\theta}{D} \cdot \left(\frac{H}{W}\right)^2$$

Where γ is the surface tension of the liquid, θ is the contact angle, D is the distance between features, and H and W are the height and width of features respectively.

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Fin Collapse Prevention

Fin complexity: Heterogeneous multi stack or encapsulated in oxide or nitride films

100% no collapse is required

Self assembled monolayer to control surface energy and contact angle

Multistep rinsing including surface derivatization and modification is Needed

Source: Patent Issued **WO 2018/063277 Al**

Inventor: Nabil Mistkawi

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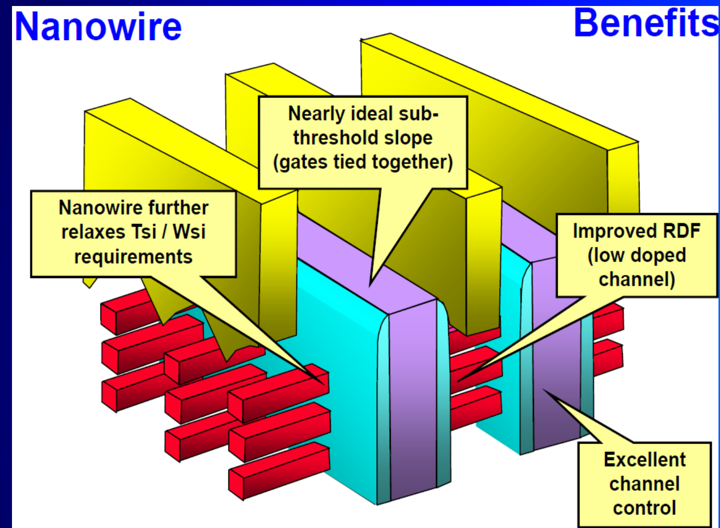
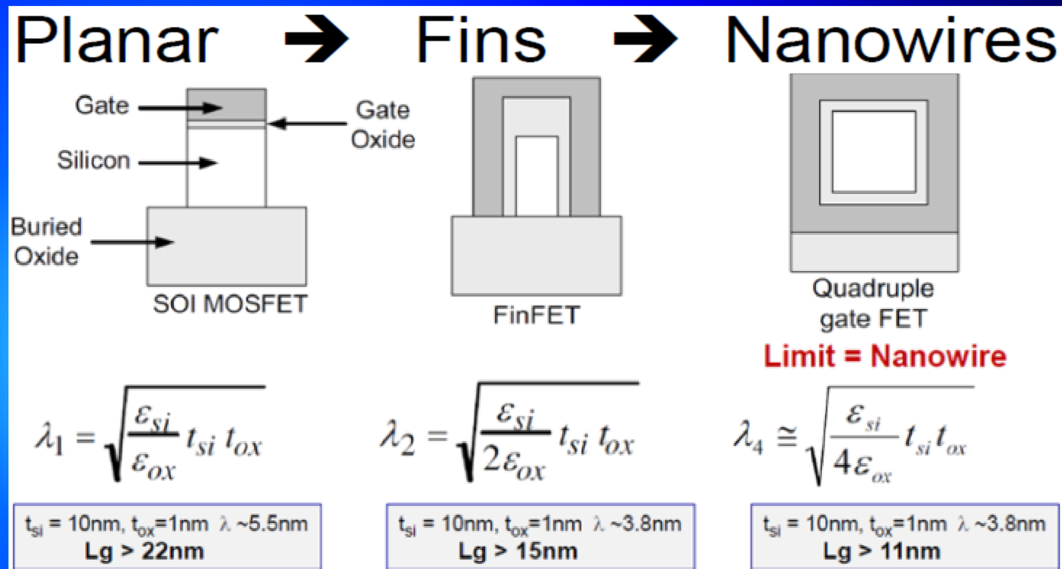
Nanowire Channel Transistor Architecture

- Gate-All-Around (GAA) currently the leading strategy for extreme scaling beyond the FinFET architecture
- Fins are replaced with Vertical stack of Si and SiGe nanowires for NMOS and PMOS transistor respectively



Source: Kelin Kuhn / ECS meeting / October 2010



> Main Motivation for NW:
- Improves short channel effects by improving device electrostatics vs. fin
- Lower I_{off} for fixed V_T (low power) Or lower V_T for fixed I_{off} (higher performance)

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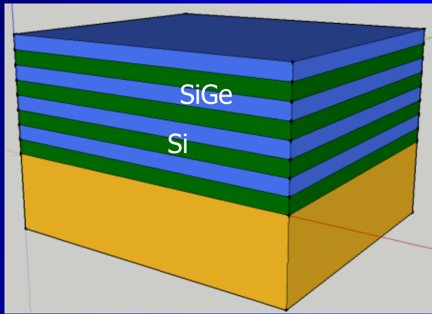
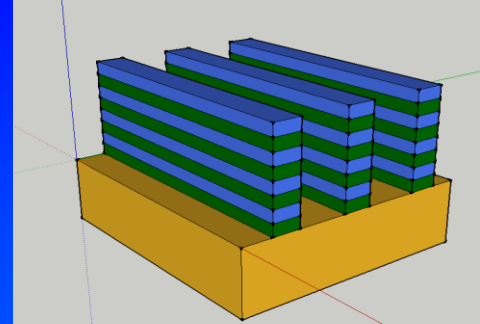
Nanowire Transistor Fabrication: Wet Etch Approach

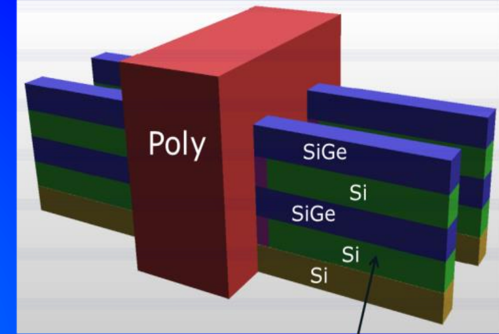
Gate-All-Around (GAA) → leading strategy for extreme scaling beyond the FinFET architecture



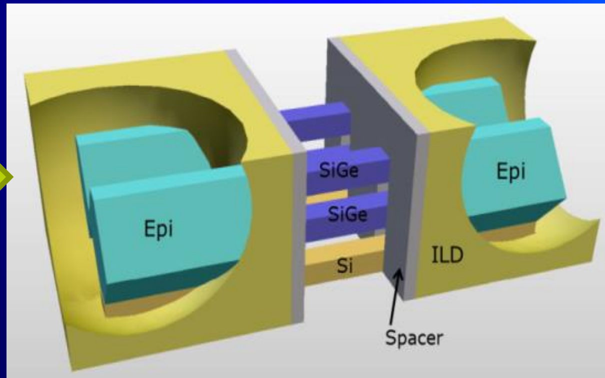
Starting Stack → Alternating Layers of Si and SiGe

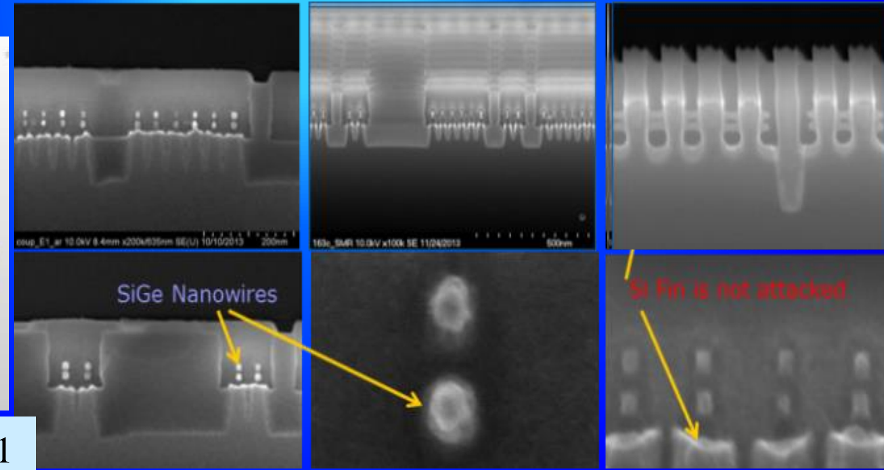


Fin Etch

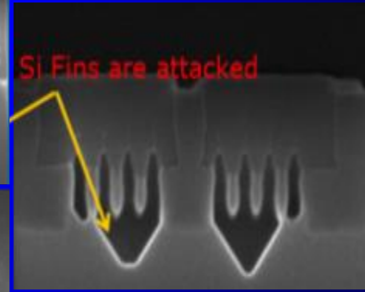


The Si (green color) must be removed selectively with respect to SiGe and ILD and horizontally to prevent Si attack (yellow color) in the downward direction.





Selectively Wet Etch

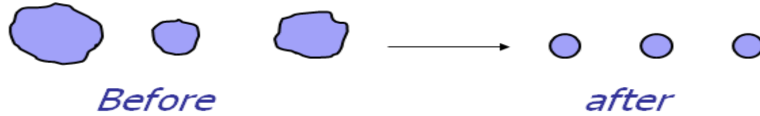


Non-Selectively Wet Etch

Source: patent issued # WO2018063300A1
Inventor: Nabil Mistkawi

What is Shot Noise in lithography patterning

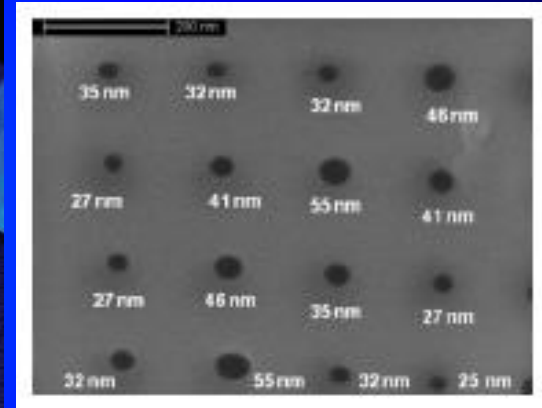
At very low dosage Critical Dimension (CD) fluctuates due to spatial fluctuations in the exposure dose



Deposit

Reflow

Etch



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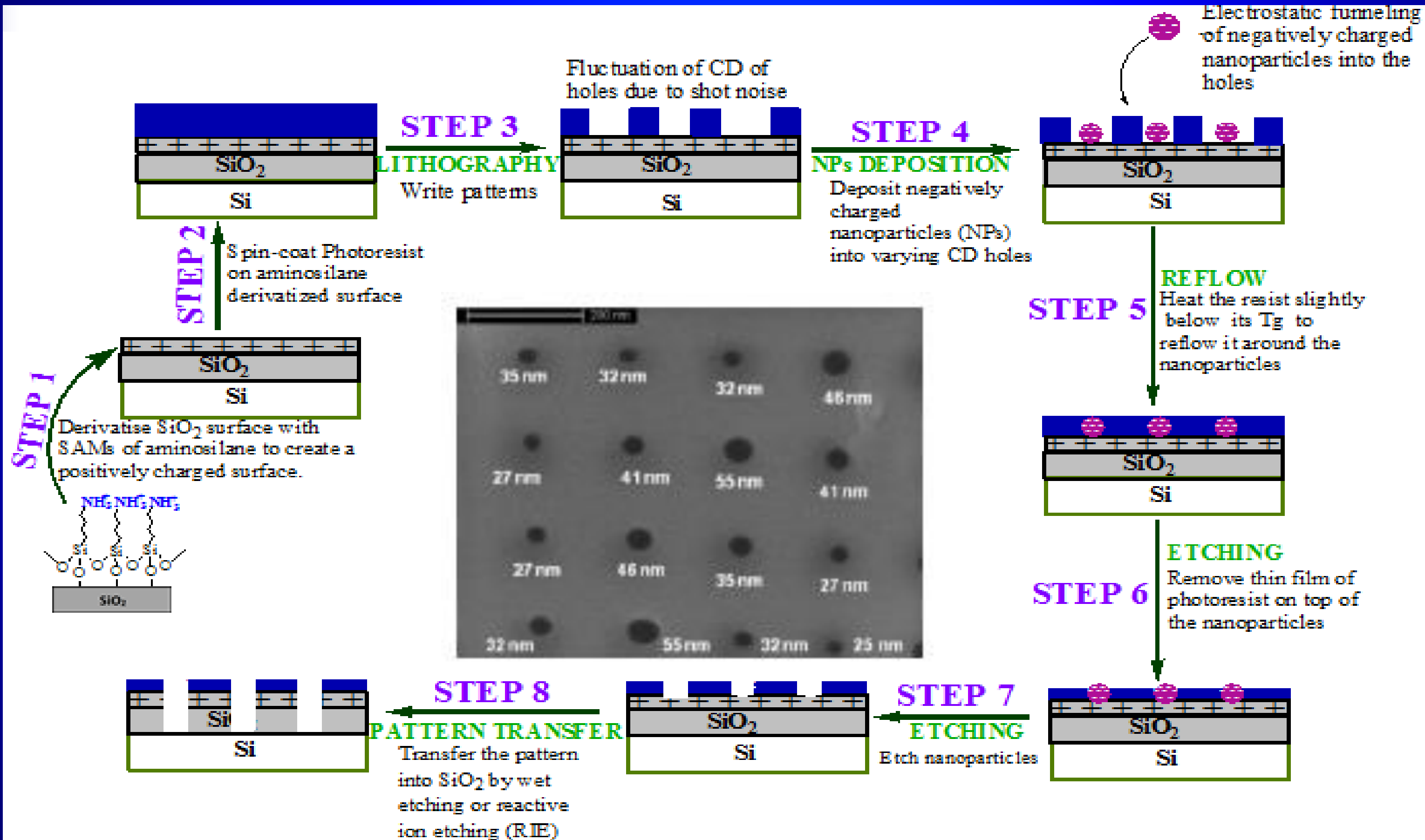
Shot Noise Mitigation Process Flow



Source: J. Mater. Chem. 100 (3), 955 2015. N. Mistkawi/PSU Collaboration

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Titanium/Titanium Nitride selective wet etch formulation Design Considerations: **Green Chemistry Approach**

At low pH only HF can dissolve Titanium.

HF also dissolves ILD (SiO_x, CDO, SiOF, Si_3N_4).

Strong oxidizers can etch titanium in the absence of HF at any pH.

W is readily etched in the presence of oxidizers.

Strategy: Take advantage of HF etching of Ti BUT figure a way to inhibit HF etching of ILD

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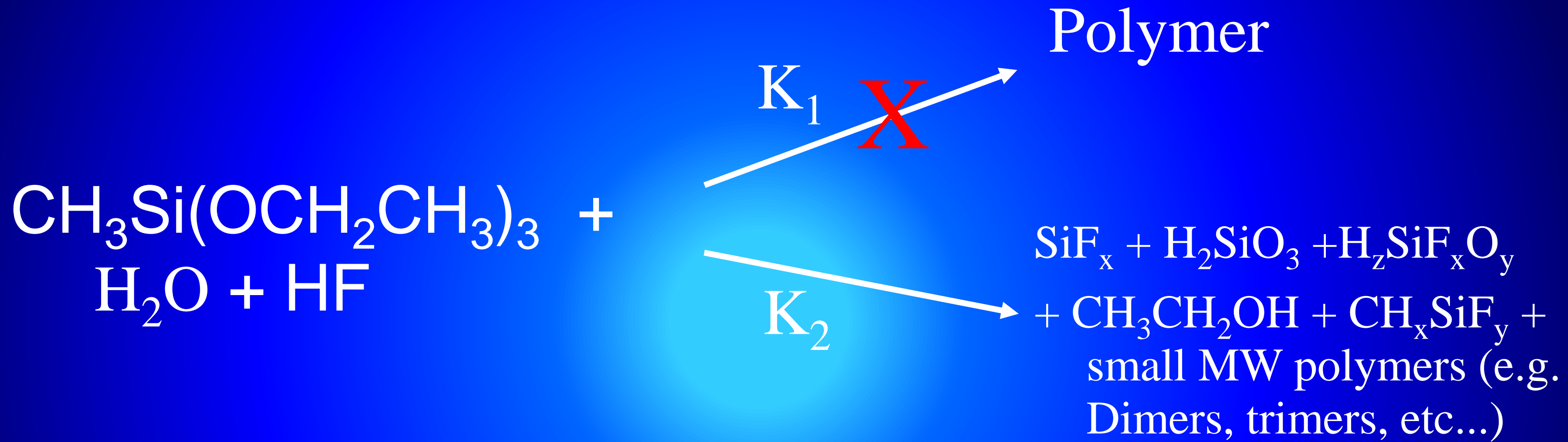
Ti/TiN selective etch formulation design Considerations



- To prevent ILD dissolution by HF, a silane coupling agent was introduced.
- Must inhibit polymer formation.

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Optimization of formulation synthesis/process cliffs & process window

MTES

49% HF

H2O

Excessive heat/Fumes

Exothermic Reaction

Low TTER

Feasible Process Window

Polymerization/ Residue on Wafers

High SiO_x ER

Surface Pitting

Particles/Oily Residue

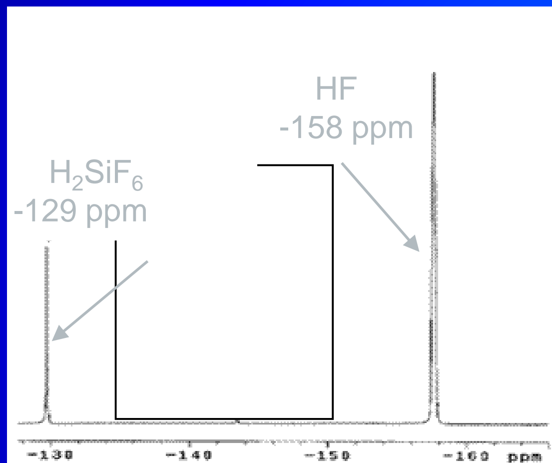
Process Window

Process Target

.1 .2 .3 .4 .5 .6 .7 .8 .9

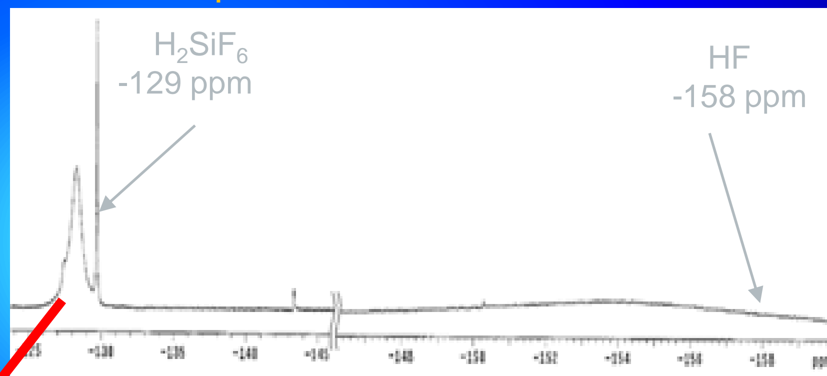
Why is the Formulation Compatible with ILD?

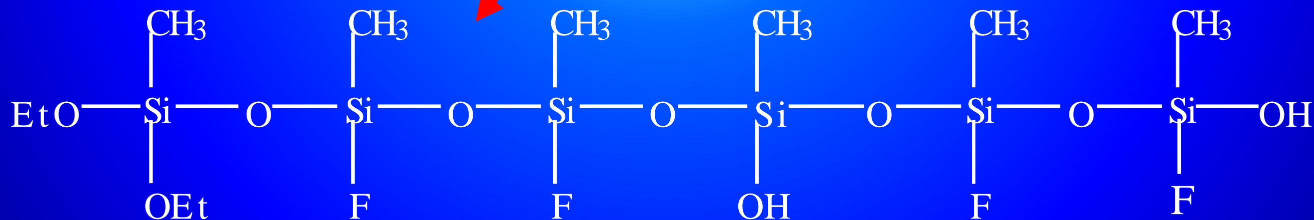
^{19}F NMR
(Dilute HF)



^{19}F NMR
(Formulation)

Distinct HF peak is absent in final formulation





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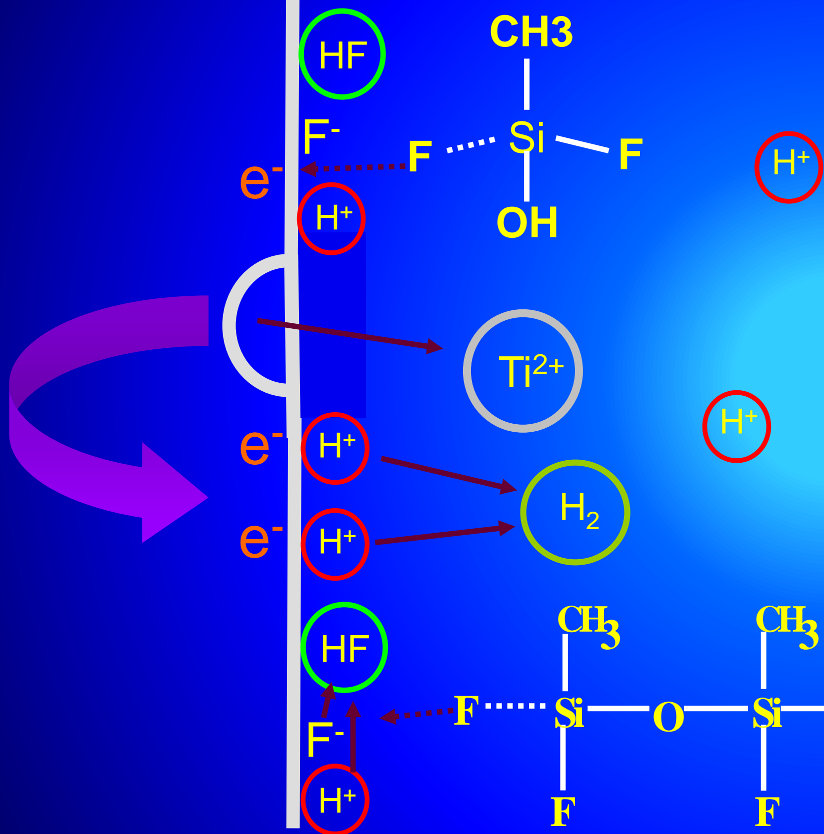
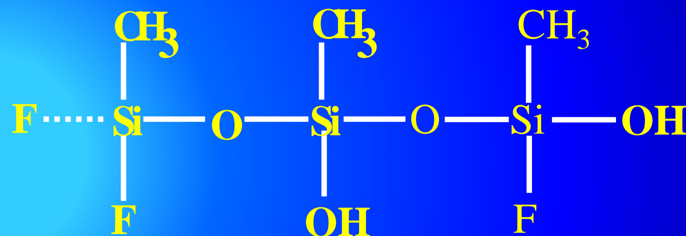
How Does it Work?



Selective Ti

Formulation Solution



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Recognitions

This work was recognized by President Obama

- **Golden Global Environmental Award**
- **LTD Award**
- **"Innovation in Technology" award by the academic community**

Two Patents Issued:

- **U.S. Patent # 8,426,319 B2**
- **U.S. Patent # 8,025,811 B2**

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Summary

- Beyond 14nm process technology nodes would require ultra pure chemicals and efficient filtration strategies
- Defect reduction, continuous yield improvements and keeping cost per transistor low is the key to the industry's success
- Contaminations and Excursions will have significant financial impact, Therefore inovative Early Detection methods are needed.
- Several promising technologies are emerging to extend moore's law into sub 10nm technology nodes:
  - Preventing pattern collapse
  - Integrating nanowire transistor channel for GAA
  - Reducing effects of short noise
  - Development of environmentally friendly wet etch chemistries

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Acknowledgments

- Colleagues at SAS
- To All SAS Suppliers: Thank You for Your Valued Partnership
- To the Linx-Consulting group, THANK YOU for the opportunity to present