SiGe selective etch for the formation of dielectric isolations in monolithic CFET

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Overview
SiGe selective etch for the formation of dielectric isolations in monolithic CFET

- Potential roadmap of logic device scaling towards CFET
- Bottom/middle dielectric isolations (BDI/MDIs)
- SiGe selective etch by commodity wet chemicals
  - Alkaline (APM) vs. acidic (FPM based) solutions
- Summary
Potential roadmap of device scaling towards CFET
Logic scaling continues with new GAA device architectures
Logic scaling enabled through disruptive device innovations

Recent progress

Nanosheet FET

Forksheet FET

Monolithic CFET

G. Bae et al. (Samsung), IEDM 2018

H. Mertens et al. (imec), VLSI 2021

S. Subramanian et al. (imec), VLSI 2020

Source: TSMC Technology Symposium 2020
Source: Intel accelerated 2021
Source: IBM press release 2021
Source: Intel press release 2021
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Bottom/middle dielectric isolations (BDI/MDIs)
Parasitic channel leakage reduction

Ground plane doping

- Off-state leakage can be reduced by ground plane doping (ion implantation before the Si/SiGe superlattice epi)

R. Ritzenthaler et al. (imec), ESSDERC 2017
Parasitic channel leakage reduction

Ground plane doping

- Off-state leakage can be reduced by ground plane doping (ion implantation before the Si/SiGe superlattice epi)

- $I_{off}$ increases with deeper SD recess and wider nanosheets

→ need for a robust solution to suppress the leakage
Parasitic channel leakage reduction
Bottom and middle dielectric isolations (BDI/MDIs)

Nanosheet FET

Forksheet FET

J. Zhang et al. (IBM), IEDM 2019

IBM press release

H. Mertens et al. (imec), VLSI 2021

H. Mertens et al. (imec), IEDM 2022

Forksheet FETs with Bottom Dielectric Isolation, Self-Aligned Gate Cut, and Isolation between Adjacent Source-Drain Structures

Parasitic channel leakage reduction
Bottom and middle dielectric isolations (BDI/MDIs)

Nanosheet FET
Forksheet FET
Monolithic CFET

J. Zhang et al. (IBM), IEDM 2019
IBM press release
H. Mertens et al. (imec), VLSI 2021
L. Van den hove (imec), SPIE 2022
Bottom/middle dielectric isolations (BDI/MDIs)

Methodology

- **Potential solution:** bottom/middle SiGe layers w/ higher [Ge] to be replaced by dielectric material(s)
BDI SiGe selective etch

Nanosheet

- **Potential solution:** bottom/middle SiGe layers w/ higher [Ge] to be replaced by dielectric material(s)

BDI SiGe selective etch (APM): SiGe50% vs. SiGe20%, and dielectric fill demonstrated
Lower Ge% in SiGe layers needed for monolithic CFET

Need to find common process window of EPI and selective etch

- Need for many Si/SiGe layers...
- Ge% reduction to avoid stress relaxation
- Need to guarantee sufficient etch contrast

mCFET Si/SiGe epi stack design requirements:
SiGe40% selective etch by APM
Selective etch SiGe40% vs. SiGe20%

APM (NH₄OH/H₂O₂/DIW)

- SiGe40%/SiGe20% multilayer stack was etched by APM with HF pre clean
- Poor selectivity to SiGe20% seen

Selectivity SiGe40%:SiGe20% ~4:1

SiGe40%/SiGe20% multilayer stack was etched by APM w/ HF pre clean

Poor selectivity to SiGe20% seen
SiGe40% selective etch by FPM based wet
Selective etch SiGe40% vs. SiGe20%  
FPM (HF/H$_2$O$_2$/DIW) vs. FPM+HCl (HF/HCl/H$_2$O$_2$/DIW)

- SiGe40%/SiGe20% multilayer stack was etched by FPM and FPM with HCl w/ HF pre-cleaning.
- Selectivity to OX and SiGe20% improved with the addition of HCl (lower pH).
Selective etch SiGe40% vs. SiGe20% by FPM+ (HF/HCl/H$_2$O$_2$/DIW)

**Impact of HF dilution**

- Higher HF conc, higher SiGe40% ER, but poorer selectivity to OX and SiGe20%
- Lower HF conc, controlled SiGe40% etch but no obvious impact on the selectivity to SiGe20%

![Image of SEM images showing OX, SiN, SiGe layers with varying HF concentrations](image-url)
Selective etch SiGe40% vs. SiGe20% by FPM+ (HF/HCl/H$_2$O$_2$/DIW)

Impact of $H_2O_2$ dilution

- Higher $H_2O_2$ conc, higher SiGe40% ER, but poorer selectivity to SiGe20%
- Lower $H_2O_2$ conc, better selectivity towards SiGe20%

![Graph showing impact of $H_2O_2$ dilution on SiGe etch rates](image)

![SEM images showing varying etch rates with $H_2O_2$ concentration](image)
Selective etch SiGe40% vs. SiGe15% by FPM+ (HF/HCl/H₂O₂/DIW)

Impact of H₂O₂ dilution

- Trade-off between SiGe40% etch rate and SiGe15% selectivity observed

With HF Pre-clean
Selective etch SiGe40% vs. SiGe15% inference

FPM* shows better selectivity towards SiGe15% compared to APM

Opportunity of wet formulations or dry etch for further selectivity improvement
SiGe selective etch opportunities

Monolithic CFET

- Opportunities of wet formulations and dry etch for SiGe selective etch
Summary
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- Logic device scaling continues with new GAA device architectures
- Dielectric isolations (BDI/MDIs) are required for monolithic CFET
- Sacrificial SiGe layers w/ higher [Ge] to be replaced by dielectric materials → need for SiGe selective etch High vs Low [Ge]
- SiGe40% selective etch vs. SiGe≤20%/Si by commodity chemicals
  - APM shows poor selectivity to SiGe20%
  - FPM selectivity to SiGe20% and OX improved with the addition of HCl (FPM⁺)
  - FPM⁺ with lower HF and H₂O₂ concentrations selectively etches SiGe40% vs. SiGe≤20%
- Opportunity of wet formulations or dry etch for further selectivity improvement
embracing a better life